BJ02

HP 71600B Series of Gbit/s Testers

Installation and Verification Manual

SERIAL NUMBERS

This manual applies directly to:

HP 70841B 0.1-3 Gbit/s Pattern Generator with serial number(s) prefixed 3136U00101.

HP 70842B 0.1-3 Gbit/s Error Detector with serial number(s) prefixed 3136U00101.

For additional important information about serial numbers, see SERIAL NUMBER INFORMATION in Chapter 1.

Serial number information for other elements in the system is contained in the following manuals:

Display - see HP 70004A Installation and Verification Manual.

Mainframe - see HP 70001A Installation and Verification Manual.

Clock Source - see HP 70311A/70312A Operating and Calibration Manual.

HEWLETT PACKARD

HP Part No. 71600-90005
Printed in U.K. December 1996

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility and to the calibration facilities or other International Standards Organization members.

WARRANTY

This Hewlett-Packard product is warranted against defects in materials and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environment specifications for the products, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

WARNING

READ THE FOLLOWING NOTES BEFORE INSTALLING OR SERVICING ANY INSTRUMENT.

1. IF THIS INSTRUMENT IS TO BE ENERGISED VIA AN AUTO-TRANSFORMER MAKE SURE THAT THE COMMON TERMINAL OF THE AUTO-TRANSFORMER IS CONNECTED TO THE NEUTRAL POLE OF THE POWER SOURCE.
2. THE INSTRUMENT MUST ONLY BE USED WITH THE MAINS CABLE PROVIDED. IF THIS IS NOT SUITABLE, CONTACT YOUR NEAREST HP SERVICE OFFICE. THE MAINS PLUG SHALL ONLY BE INSERTED IN A SOCKET OUTLET PROVIDED WITH A PROTECTIVE EARTH CONTACT. THE PROTECTIVE ACTION MUST NOT BE NEGATED BY THE USE OF AN EXTENSION CORD (POWER CABLE) WITHOUT A PROTECTIVE CONDUCTOR (GROUNDING).
3. THE SERVICE INFORMATION FOUND IN THIS MANUAL IS OFTEN USED WITH POWER SUPPLIED TO AND PROTECTIVE COVERS REMOVED FROM THE INSTRUMENT. ENERGY AVAILABLE AT MANY POINTS MAY, IF CONTACTED, RESULT IN PERSONAL INJURY.
4. BEFORE SWITCHING ON THIS INSTRUMENT:
   a. Make sure the instrument input voltage selector is set to the voltage of the power source.
   b. Ensure that all devices connected to this instrument are connected to the protective (earth) ground.
   c. Ensure that the line power (mains) plug is connected to a three-conductor line power outlet that has a protective (earth) ground. (Grounding one conductor of a two-conductor outlet is not sufficient).
   d. Check correct type and rating of the instrument fuse(s).
5. SERVICING INFORMATION:
   a. This manual contains information, cautions and warning which must be followed to ensure safe operation and to retain the instrumnet in safe condition. Service and adjustments should be performed only by qualified service personnel.
   b. Any adjustment, maintenance and repair of the opened instrument under voltage should be avoided as much as possible and, when unavoidable, should be carried out only by a skilled person who is aware of the hazard involved.
   c. Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.
   d. Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.

HP 71600 Series Overview

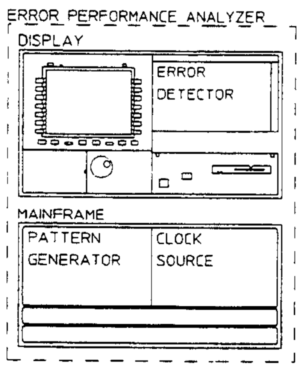
Introduction

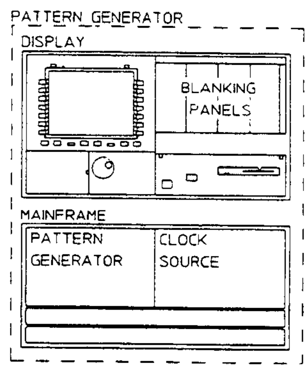
The HP 71600 Series can be configured into one of the following:

HP 71603B 0.1-3 Gbit/s Error Performance Analyzer
HP 71604B 0.1-3 Gbit/s Pattern Generator

Systems Overview

The basic systems are shown in the following illustrations:





The elements which make up your system are identified by product number in the following table:

Element	HP 71603B Error Performance Analyzer	HP 71604B Pattern Generator
Display	HP 70004A	HP 70004A
Mainframe	HP 70001A	HP 70001A
Pattern Generator	HP 70841B	HP 70841B
Error Detector	HP 70842B	-
*Clock Source	HP 70311A	HP 70311A

*Clock Source is not supplied if Option 100 is ordered with your system, see *Options* on page 1-2 for more detail.

Documentation Overview

The manuals which are supplied with each system are listed in the following table:

Element	Product Number	Manual	HP Part Number	Comments
System	HP 71603B HP 71604B	Installation/Verification Operating Programming	71600-90005 71600-90004 71600-90006	These manuals are supplied with all systems.
Display	HP 70004A	Operation Installation/Verification	70004-90031 70004-90005	These manuals are supplied with all systems.
Mainframe	HP 70001A	Installation/Verification	70001-90021	This manual is supplied with all systems operating as Error Performance Analyzers.
*Clock Source	HP 70311A HP 70312A	Operating/Calibration	70311-90000	This manual is supplied with all systems.

Service manuals covering the elements in your system are listed in the following table:

Element	Product Number	Service Manual HP Part Number	Comments
System	HP 71603B HP 71604B	71600-90009	This manual is required for all systems.
Display	HP 70004A	70003-90009	This manual is required for all systems.
Maindrame	HP 70001A	70001-90044	This is manual required for systems operating as an Error Performance Analyzer.
*Clock source	HP 70311A HP 70312A	70311-90001	This manual is required for all systems.

*Clock Source documentation is not supplied if Option 100 is ordered with your system, see *Options* on page 1-2 for more detail.

HP 71600 Series Installation and Verification Manual

This manual is shipped from the factory with only the system installation and verification information.

When the display and Mainframe Installation and Verification Manuals are unpacked they should be inserted into the *HP 71600 Series Installation and Verification Manual*, (all installation and verification information is then contained within the one binder).

User Tasks

Listed below are typical user tasks and chapter references:

Task	Chapter
Getting the system ready for use.	Installation2
Identifying error conditions and messages	Troubleshooting 5
Verifying the system meets specification.	Performance Tests 4
Understanding a master/slave Modular Measurement system.	HP 71600 Series (MMS) 6
Understanding a master/master Modular Measurement System.	Appendix A
Controlling the system remotely through HP-IB	HP-IB 7

Printing History

The Printing History shown below lists all Editions and Updates of this manual and the printing date(s). The first printing of this manual is Edition 1. The Edition number increments by 1 whenever the manual is revised. Updates, which are issued between Editions, contain replacement pages to correct the current Edition of the manual. Updates are numbered sequentially starting with Update 1. When a new Edition is created, it contains all the Update information for the previous Edition. Each new Edition or Update also includes a revised copy of this printing history page. Many product updates or revisions do not require manual changes and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one-to-one correspondence between product updates and manual updates.

Edition 1 (71600-90005)	December 1991
Edition 2 (71600-90005)	March 1992
Edition 3 (71600-90005)	December 1996

Contents

1

General Information

Introduction

This chapter contains general information about the HP 71600 Series System and is divided into the following sections:

Options	Lists all the options available with your system.
Accessories Supplied	Lists the accessories supplied with your system.
Serial Number Information	Explains the Hewlett-Packard serial numbering system.
Returning Modules for Service	Contains information on how to return a module to Hewlett-Packard for service.
Precautions	Highlights electrostatic discharge procedures and accessories available. This section also contains information on cleaning the display.

Options

The options which may have been ordered with your system are listed below:

Option 100 Deletes the Clock Source module and adds four 1/8 blanking panels for the *Error Performance Analyzer* system.

Deletes the Clock Source module, Mainframe, four 1/8 blanking panels and two HP-MSIB cables for the *Pattern Generator* system.

Option 200 Delete the HP 15680A RF Accessory Kit.

Option 908 Rack mount flanges for systems without handles fitted.

Option 910 Extra set of manuals - provides an additional set of installation/verification and operating manuals for your system.

Option 913 Rack mount flanges for systems with handles fitted.

Option + W30 Two years additional hardware support beyond the standard one-year warranty.

Accessories Supplied

The accessories supplied with your system are listed below:

- HP 15680A RF Accessory Kit.
- Two HP-MSIB cables.
- Two Line power cables.
- 8 mm hex-ball driver.
- Four 1/8 blanking panels (HP 5061-9006) - required for the Display in the *Pattern Generator* system.
- HP 70841-60049 N-type cable (not supplied when Option 100 is ordered).

Serial Number Information

Attached to each element in your system is a serial number plate. A typical serial number is in the form XXXXUXXXXX. It is in two parts; the first four digits and the letter are the serial prefix and the last five are the suffix, the letter designates the country of origin - U is the United Kingdom. The prefix is the same for identical elements, it only changes when a change is made to an element in your system. The suffix however, is assigned sequentially and is different for each element. The contents of this manual apply to the elements with the serial number prefix(es) listed under *SERIAL NUMBERS* on the title page.

A system manufactured after the printing of this manual may have a number prefix that is not listed on the title page. The unlisted serial number prefix indicates the system is different from those described in this manual. The manual for this new element is accompanied by a *Manual Changes* supplement. This supplement contains *change information* that explains how to adapt the manual to the new element.

In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complementary copies of the supplement are available from Hewlett-Packard. For information concerning a serial number prefix that is not listed on the Manual Changes supplement, contact your nearest Hewlett-Packard office.

Returning Modules for Service

This section explains how you return a module to Hewlett-Packard for servicing.

Packaging Requirements

Instruments and modules can be damaged as a result of using packaging materials other than those specified. Never use styrene pellets as packaging material. They do not adequately cushion the instrument nor prevent it from shifting in the carton. They also cause instrument damage by generating static electricity.

Preparing a Module for Shipping

1. Fill out a blue repair tag (located at the front of this manual) and attach it to the instrument or module. Include any error messages or specific performance data related to the problem. If a blue tag is not available, the following information should be noted and sent with the module or instrument:
   - Type of service required.
   - Description of the problem.
   - Whether problem is constant or intermittent.
   - Name and phone number of technical contact person.
   - Return address.
   - Model number of returned module or instrument.
   - Full serial number or returned module or instrument.
   - List of any accessories returned with the module or instrument.
2. Pack the module or instrument in the appropriate packaging materials. Original shipping or equivalent materials should be used. If the original or equivalent material cannot be obtained, follow the instructions below:

Caution Inappropriate packaging of the instrument may result in damage to the instrument during transit.

- Wrap the instrument in anti-static plastic to reduce the possibility of damage caused by ESD.
- Use a double-walled, corrugated cardboard carton of 159 kg (350 lb) test strength.

Caution If you are shipping a complete system, remove the module(s) from Display and Mainframe, individually pack each element, then ship them to Hewlett-Packard.

- The carton must be large enough to allow 3- to 4-inches on all sides of the instrument for packing material and strong enough to accommodate the weight of the instrument.
- Surround the instrument with 3- to 4-inches of packing material, to protect the instrument and prevent it from moving in the carton.
- If packing foam is not available, the best alternative is S.D.-240 Air Cap™ from Sealed Air Corporation (Commerce, California 90001). Air Cap™ looks like a plastic sheet filled with air bubbles.
- Use the pink (anti-static) Air Cap™ to reduce static electricity. Wrapping the instrument several times in this material will protect the instrument and prevent it from moving in the carton.

3. Seal the carton with strong nylon adhesive tape.
4. Mark the carton *FRAGILE, HANDLE WITH CARE.*
5. Retain copies of all shipping papers.

Precautions

ESD Precautions

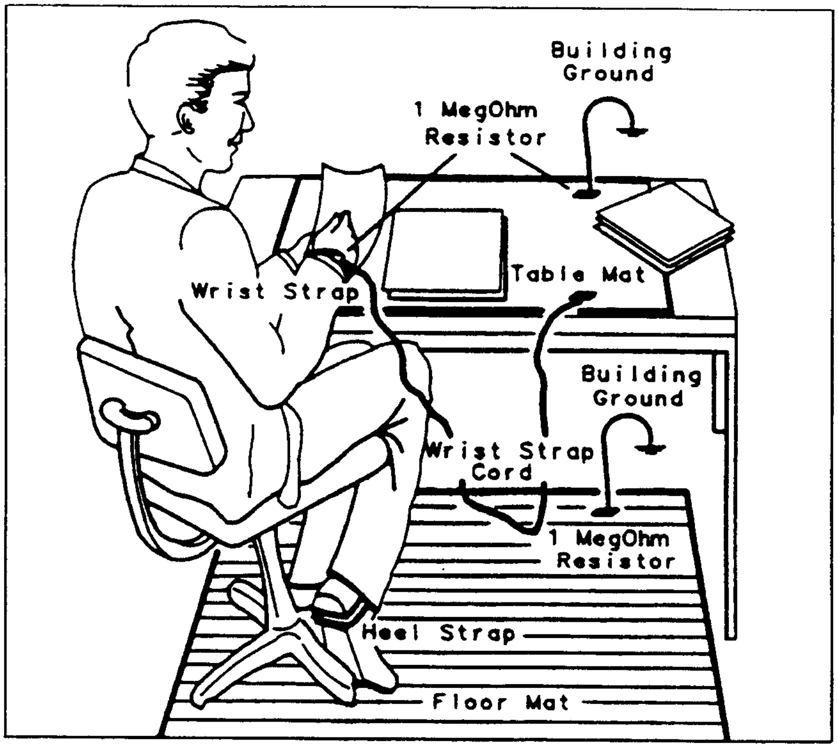
Electrostatic discharge (ESD) can damage or destroy electronic components. All work on electronic assemblies should be performed at a static-safe workstation.

Static-safe Workstation

A typical static-safe workstation is illustrated in the following diagram. There are two types of ESD protection:

- Wrist-strap (with > 1 MΩ isolation to ground) with table-mat.
- Heel-strap (with > 1 MΩ isolation to ground) with conductive floor-mat.

These two types must be used together to ensure adequate ESD protection. Isolation to ground must be provided for personnel protection.



Static-safe Accessories

The following table lists the accessories that may be ordered through any Hewlett-Packard sales and service office.

HP Part Number	Description
9300-0797	3M static control mat 0.6 m x 1.2 m (2 ft x 4 ft) and 4.6 m (15 ft) of ground wire. (The wrist-strap and wrist-strap cord are not included. They must be ordered separately.)
9300-0980	Wrist-strap cord 1.5 m (5 ft).
9300-1383	Wrist-strap, color black, stainless steel, has four adjustable links and a 7 mm post-type connection.
9300-1169	ESD heel-strap (reusable 6- to 12- months).
*92175A	Black, hard surface, static control mat, 1.2 m x 1.5 m (4 ft x 5 ft)
*92175B	Brown, soft surface, static control mat, 1.2 m x 2.4 m (4 ft x 8 ft)
*92175C	Small, black, hard surface, static control mat, 0.9 m x 1.2 m (3 ft x 4 ft)
*92175T	Table-top static control mat, 58 cm x 76 cm (23 in x 30 in)
*92176A	Natural color anti-static carpet, 1.2 m x 1.8 m (4 ft x 6 ft)
*92176B	Natural color anti-static carpet, 1.2 m x 2.4 m (4 ft x 8 ft)
*92176C	Russet color anti-static carpet, 1.2 m x 1.8 m (4 ft x 6 ft)
*92176D	Russet color anti-static carpet, 1.2 m x 2.4 m (4 ft x 8 ft)

*Can also be ordered by calling HP DIRECT Phone (800) 538 8787.

Display Cleaning

To avoid damaging the coating on the display, use a thin-film cleaner such as Hewlett-Packard Video Clean Kit (HP part number 92193). The kit includes an non-abrasive cleaning cloth.

Caution

Hand and laboratory paper towels are abrasive, if these are used they may damage the coating on the display.

2

Installation

This chapter enables you to install your system ready for use. The information is presented under the following headings:

Preparation for Use	Provides information you should read before you install your system. It contains information on initial inspection, power requirements, address switches and rack mount kits.
System Installation	Shows you how to install your system. As you progress through the procedure, you will be directed to other relevant information.
System Verification	Describes how you power-on and verify correct system installation, and directs you to troubleshooting (if there are any problems).
Selftest at Power-on	Details the instrument status during selftest at power-on.
Installing/Removing Modules	Describes how you install modules into a Display and Mainframe.

Preparation for Use

This section should be read before you install your system. It contains the following:

- Initial Inspection
- Operating Requirements
- Line Voltage Selection
- Line Fuses
- Power Cables
- HP-MSIB Address Switches
- HP-IB Address Switches
- Bench Operation
- Rack Mount Kits

Initial Inspection

Warning **To avoid hazardous electrical shock, do not perform electrical tests when there are signs of shipping damage to any portion of the outer enclosure (covers, panels, meters).**

Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents of the shipment have been checked for completeness and the elements in your system have been checked both mechanically and electrically. Procedures for checking the electrical operation are given in chapter 4 of this manual.

If any element in your system appears damaged or is defective, contact the nearest Hewlett-Packard service office. Hewlett-Packard will arrange for repair or replacement of the equipment without waiting for a claim settlement. Retain the shipping materials for the carrier to inspect.

Mainframes and stand-alone instruments such as the HP 70004A Display, are shipped with the front handles attached.

Undamaged shipping materials should be kept. Original HP or equivalent shipping materials are required for system or module re-shipment, as substandard packaging may result in damage. Refer to *Returning Modules for Service* in chapter 1 for information on re-shipment.

Operating Requirements

Operating and Storage Environment

The system may be operated in temperatures from 0 °C to +45 °C. For storage, the temperature range is −40 °C to +65 °C.

The system should be protected against temperature extremes which may cause condensation within the elements in your system.

Physical Specifications

The physical dimensions and weight of each element in your system are contained in chapter 3 *Specifications*.

Power Requirements

The line voltage requirements for the Display and Mainframe are as follows:

115 V line operation: 90 to 132 V ac, 47 to 66 Hz
230 V line operation: 198 to 264 V ac, 47 to 66 Hz

The maximum power consumption is as follows:

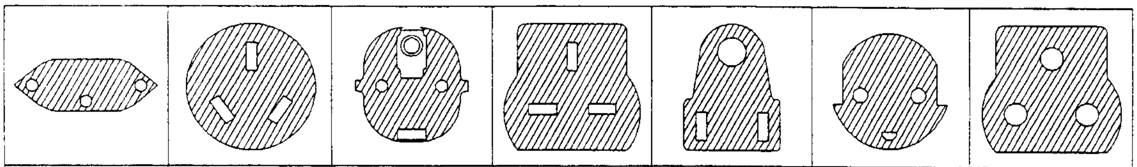
Display	260 W maximum, 350 VA maximum
Mainframe	310 W maximum, 570 VA maximum

Warning **Before turning the system on, make sure it is grounded through the protective conductor of the power cable to a socket outlet with protective earth contact. Any interruption of the protective (grounding) conductor inside or outside the instrument, or disconnection of the protective earth terminal, can result in personal injury.**

Power Cables

The Display, Mainframe and Clock Source are equipped with a three-wire power cable. When connected to a properly grounded power outlet, this cable grounds the instrument case.

The power cable shipped with each instrument depends on the country of destination. The plug configuration and the power cable part numbers are listed below. If the appropriate power cable(s) are not supplied with your system or are damaged, notify the nearest Hewlett-Packard sales and service office and replacement(s) will be provided.



8120-2104	8120-1369	8120-1689	8120-1351	8120-1378 US 8120-4753 JAP	8120-2956	8120-4211

The color code used in each power cable is given below:

Line	Brown
Neutral	Blue
Ground	Green/yellow

Line Voltage Selection

Display (HP 70004A) Line Voltage Selector

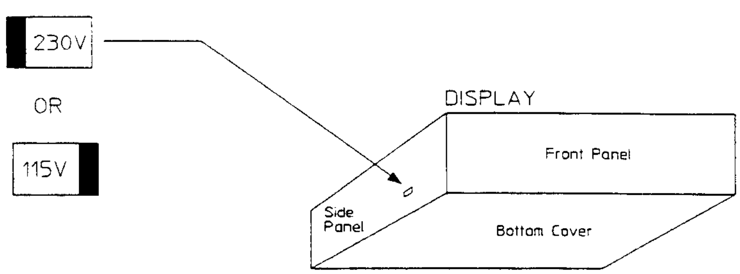
Caution

Before you connect the power cable to the Display, check that the LINE VOLTAGE SELECTOR switch is set for the correct line voltage source.

If the wrong voltage is selected, one of the following may happen:

If 115 V line operation is selected and you connect to a 230 V ac line power source, the fuse may blow.
If 230 V line operation is selected and you connect to a 115 V ac line power source, the instrument will not power-on correctly.

The LINE VOLTAGE SELECTOR slide switch is located through a slot in the left side-panel.



Mainframe (HP 70001A) Line Voltage Selector

Caution

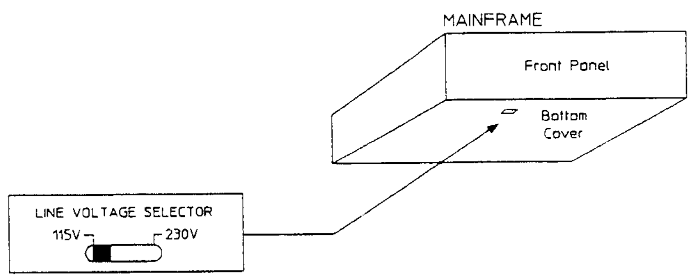
Before you connect the power cable to the Mainframe, check that the LINE VOLTAGE SELECTOR switch is set for the correct line voltage source.

If the wrong voltage is selected, one of the following may happen:

If 115 V line operation is selected and you connect to a 230 V ac line power source, the fuse may blow.

If 230 V line operation is selected and you connect to a 115 V ac line power source, the instrument will not power-on correctly.

The LINE VOLTAGE SELECTOR slide switch is located through a slot in the bottom panel (the switch is set for 115 V operation in the above diagram).



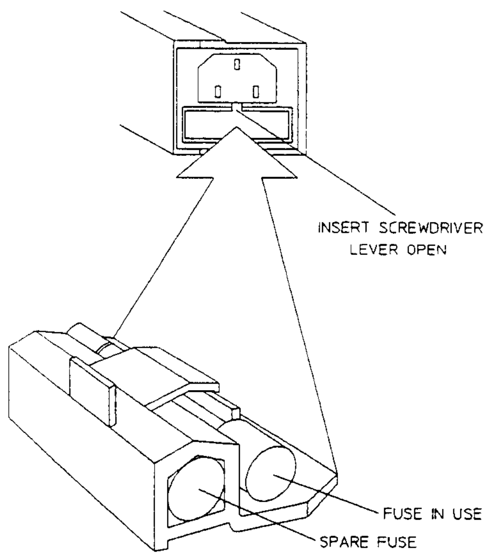
Line Fuses

The line fuses of the Display, Mainframe and Clock Source are located in the line-module housings on the rear panel.

Accessing the Display (HP 70004A) and Mainframe (HP 70001A) Fuses

The Display and Mainframe use similar line-module housings (see the following diagram). To access the fuses:

1. Ensure no power cable is connected to the line-module housing.
2. Use a screwdriver to lever open the fuse holder. A spare line fuse is located inside the fuse holder.



Fuse Ratings

The fuse ratings and the part numbers for 115 V ac and 230 V ac operation are listed below:

The Display and Mainframe fuse rating are 6.3 A, 250 V (HP 2110-0703) for both 115 and 230 V ac operation.

HP-MSIB Address Switches

The HP-MSIB address switches are factory preset to configure your *Error Performance Analyzer* or *Pattern Generator* as a master/slave Modular Measurement System (MMS).

If you want to change the master/slave addressing or want to change to master/master configuration, ensure you are fully aware of the HP-MSIB address protocol, see chapter 6.

In an Error Performance Analyzer system the Error Detector master module controls the slave Pattern Generator module and the Clock Source. The Pattern Generator module (a slave to the Error Detector) is a sub-master to the Clock Source. The Clock Source is controlled directly by the Pattern Generator, and indirectly by the Error Detector (through the Pattern Generator).

In a Pattern Generator system the master module is the Pattern Generator, it controls the slave Clock Source.

Factory Preset HP-MSIB Addresses

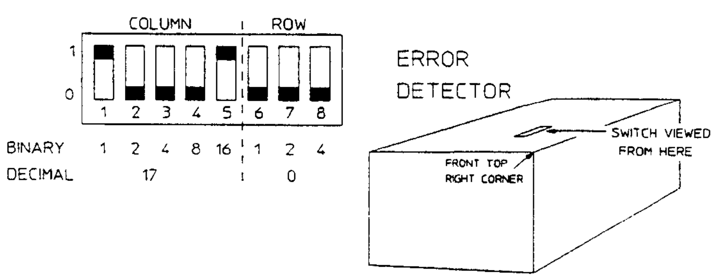
The factory preset HP-MSIB addresses (row,column) are listed below:

Display	: 0, 20
Error Detector	: 0, 17*
Pattern Generator	: 1, 18 (for the *Error Performance Analyzer*)
	: 0, 18* (for the *Pattern Generator* system)
Clock Source	: 2, 19

* Column value defines the factory preset HP-IB addresses.

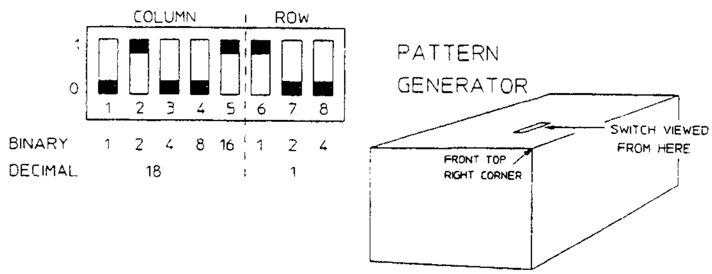
Error Detector Module Address Switches

These are accessed through a slot on top of the module. The factory preset settings are shown in the following diagram:



Pattern Generator Module Address Switches

These are accessed through a slot on top of the module. The factory preset settings for a Pattern Generator module in an *Error Performance Analyzer* system are shown in the following diagram:

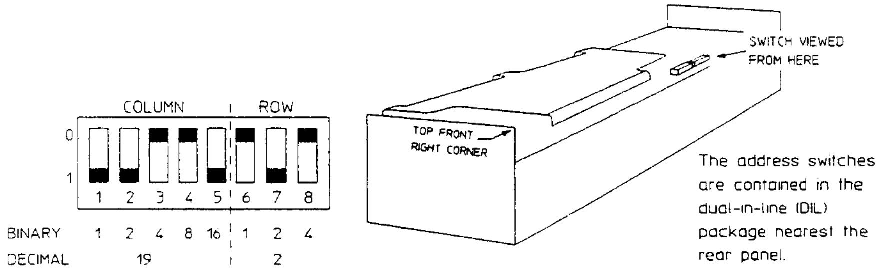


Note

The factory preset settings for a Pattern Generator module in a *Pattern Generator* system are (0, 18).

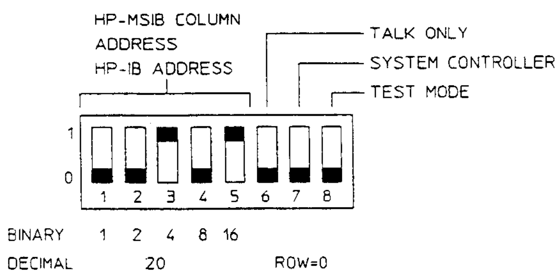
Clock Source Module Address Switches

These switches are housed in a dual-in-line (DIL) package, the factory preset switch settings and location are shown in the following diagram:



Display Address Switches

These are located on the rear panel of the HP 70004A Display, it has no row switches (it defaults to row 0) - only column switches (the factory preset settings are shown in the following diagram):



HP-IB Address Switches

The HP-MSIB address switches in a master module (Error Detector or Pattern Generator) also act as HP-IB switches. If you want your system to communicate over the HP-IB:

The *row* switches must be set to *0*.

The *column* switches define the *HP-IB* address.

If you want to change the HP-IB address (ie, use an address that is different from that defined by the *column* switch settings), it is recommended that you use the Display *HP-IB Address* function, see the *HP 71600 Series Operating Manual*.

Caution It is not recommended that you change the HP-IB address using the HP -MSIB/HP-IB switches, as these also change the HP-MSIB address. If the HP-MSIB address protocol is violated your system will fail to operate.

Factory Preset HP-IB Addresses

The Error Detector HP-IB address is factory preset to 17 (column part of HP-MSIB switch setting).

The Pattern Generator HP-IB address is factory preset to 18.

Bench Operation

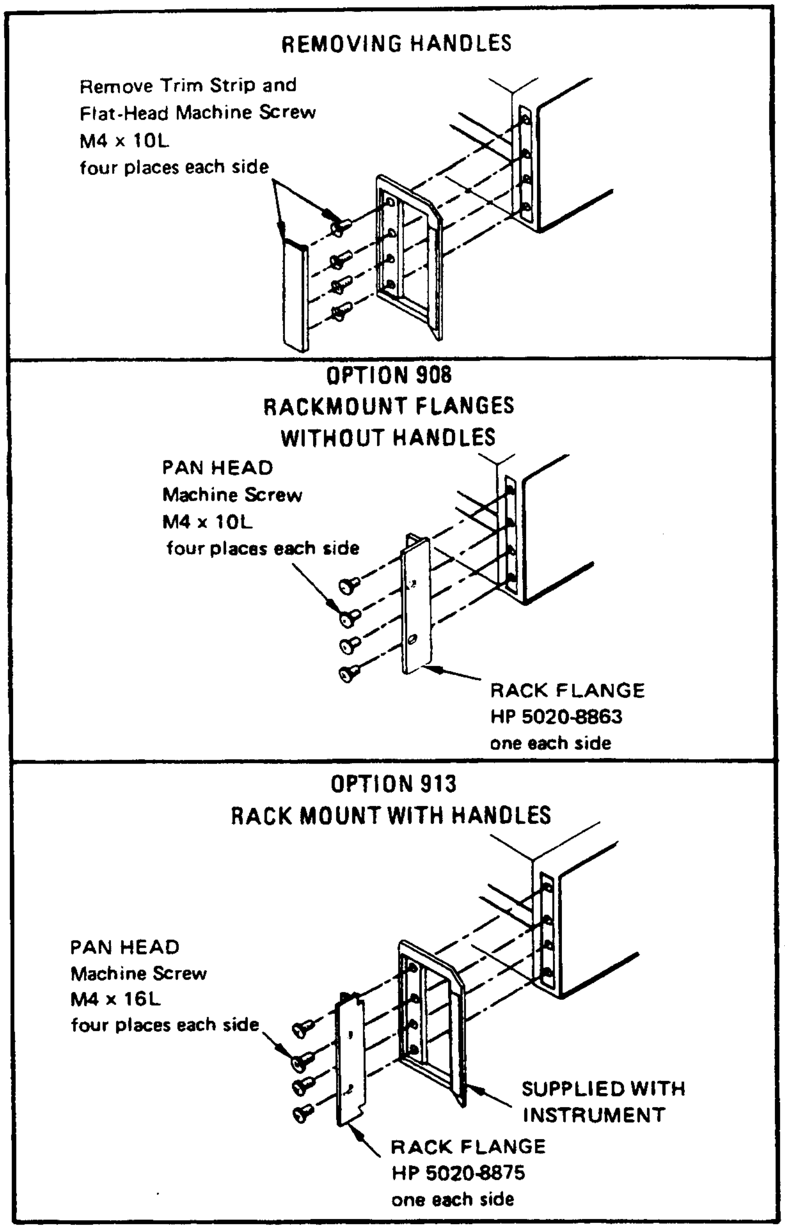
Plastic feet are included with Mainframes and stand-alone instruments to provide bench operation convenience. The plastic feet are self-aligning when systems are to be stacked.

Rack Mount Installation

Front handles must be removed when fitting the system rack mount options.

The rack mounts that are available are illustrated in the diagram on page 2-11. Angled brackets (HP 12679C) may be ordered to provide additional rear or side support for the rack mounted instruments. The table below lists the rack mount kit part numbers.

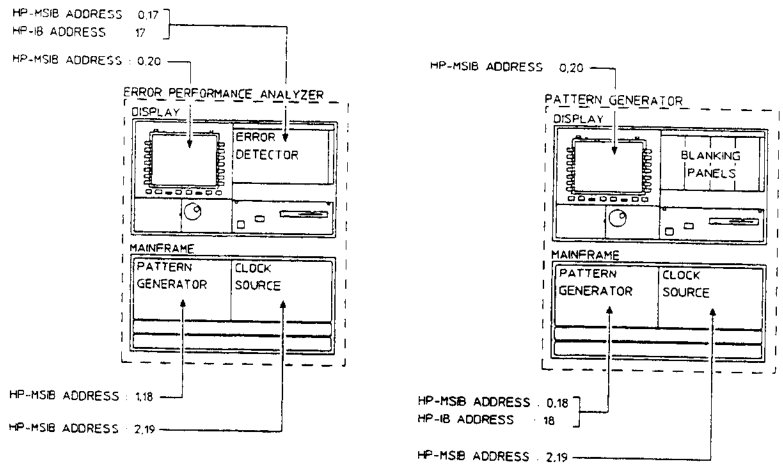
Device	Rack Mount Kit	
	Option 908	**Option 913**
Display	HP 5062-3979	HP 5062-4073
Mainframe	HP 5062-3978	HP 5062-4072



NOTE: LEFT FRONT IS SHOWN IN EACH EXAMPLE.

System Installation

Your HP 71600 Series can be installed to operate as an *Error Performance Analyzer* or as a *Pattern Generator* system.



Use the following table to identify the elements (by product number) which make up your system:

Element	HP 71603B Error Performance Analyzer	HP 71604B Pattern Generator
Display	HP 70004A	HP 70004A
Mainframe	HP 70001A	HP 70001A
Pattern Generator	HP 70841B	HP 70841B
Error Detector	HP 70842B	-
*Clock Source	HP 70311A	HP 70311A

* Clock Source is not supplied if Option 100 is ordered with your system, see *Options* on page 1-2 for more detail.

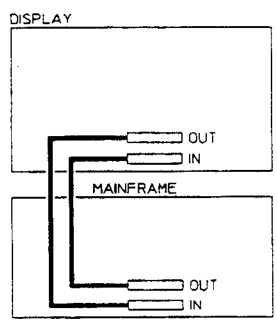
Caution Ensure that no power cables are connected. Also check that the LINE power switches are set to off.

Procedure

Caution Ensure that the Display and Mainframe line voltage selector switches are set for the line voltage being used, also check the fuse ratings, see pages 2-4 and 2-6.

1. Use the factory preset HP-MSIB and HP-IB addresses to install the Display and Modules as a master/slave system, see the diagram on the previous page and pages 2-7 to 2-10.
2. If your system is an Error Performance Analyzer, install your *Error Detector* module into the Display, see page 2-20.
3. If your system is a Pattern Generator, install 4 blanking panels into the Display.
4. Install your Pattern Generator module into the left side of the Mainframe and Clock Source module into the right side, see page 2-21.
5. Arrange the elements which make up your system for bench operation. The plastic feet on the Display and Mainframe are self aligning when systems are stacked. To rack mount your system, refer to *Rack Mount Installation*, see page 2-10.
6. Connect the HP-MSIB cables as follows:

Caution Your system must be powered down when connecting or disconnecting HP-MSIB cables.



The diagram shows the systems viewed from the rear.

7. Connect the *CLOCK IN* port of the Pattern Generator module to the *CLOCK OUT* of the Clock Source module, using the accessory cable HP 70841-60049.

Note

The other front panel ports on the Pattern Generator and Error Detector modules are interconnected according to the application you want to undertake. Accessory Kit HP 15680A contains the necessary cables, adapters and 50Ω terminations. Unused ports must be terminated in 50Ω.

8. Connect the two power cables to your system then connect the cables to the power outlets.

Caution

Check the power cables for damage before powering on your system, see the *Power Cables* on page 2-4.

Your system is now ready for *System Verification*, see page 2-15.

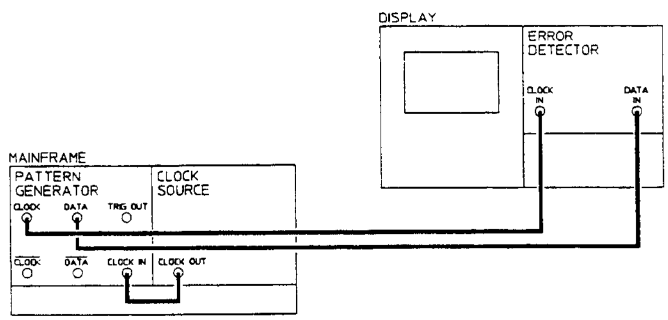
System Verification

This section contains procedures which will enable you to verify that your *Error Performance Analyzer* (see this page) or *Pattern Generator* system (see page 2-17) has been correctly installed.

Error Performance Analyzer System Verification

The Error Detector and Pattern Generator modules are connected back-to-back, then the system selftest and instrument preset parameters are used to verify correct installation. A description of what you will see during selftest is given in *System Selftest at Power-on*, see page 2-19 (since selftest takes only 15 seconds approximately to complete, you should read the description before powering on your system).

1. Interconnect the front panel ports as shown below, then prior to switching on your system, read *Selftest at Power-on* on page 2-19.

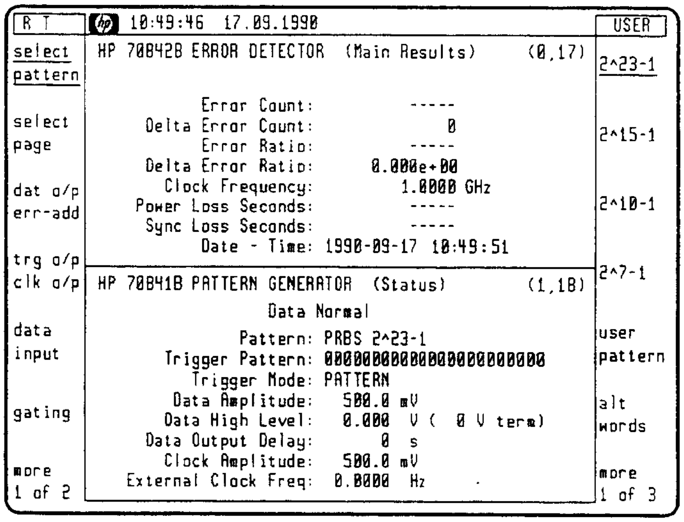


Note : All unused Pattern Generator and Error Detector ports must be terminated in 50Ω

The HP 15680A RF Accessory Kit contains the 50Ω terminations.

2. Switch on the two *Line* power switches (in any order) - wait approximately 15 seconds for selftest to end.

3. Press the Display (INST PRESET) key to set up the instrument preset parameters. The display should be as follows:



4. Check that the displayed clock frequency is 1 GHz and that the *ACT* indicators on all modules are lit.

5. Press the Display (DISPLAY) key, the *ACT* indicators should extinguish and an *A* should appear at the top left of the display.

6. Press the Display (MENU) key, the *A* should disappear and the *ACT* indicators should light.

7. Press **data input** then **more 1 of 2** (right menu). Press **CLK-DAT ALIGN** then wait a few seconds for the clock and data signals to align (see *HP 71600 Series System Operating Manual*).

8. Press **gating** followed by **RUN GATING**. The *GATING* indicator on the Error Detector should light.

9. Check that the displayed error count is 0.

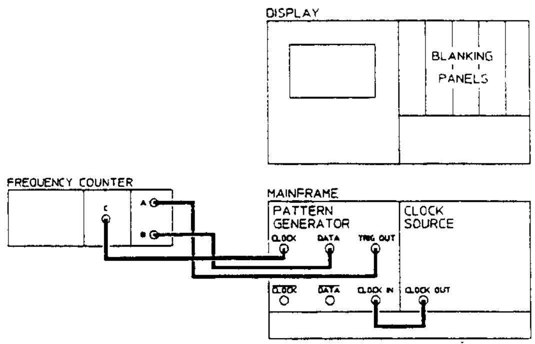
If the system does not operate as described (ie, selftest fails or error indicators are lit after selftest), go to the troubleshooting in chapter 5.

If there are no errors, the system is ready for use.

Pattern Generator System Verification

The Pattern Generator is connected to a counter, then the system selftest and instrument preset parameters are used to verify correct installation. A description of what you will see during selftest is given in *System Selftest at Power-on*, see page 2-19 (since selftest takes only 15 seconds approximately to complete, you should read the description before powering on your system).

1. Interconnect the front panel ports as shown below, then prior to switching on your system, read *Selftest at Power-on* on page 2-19.

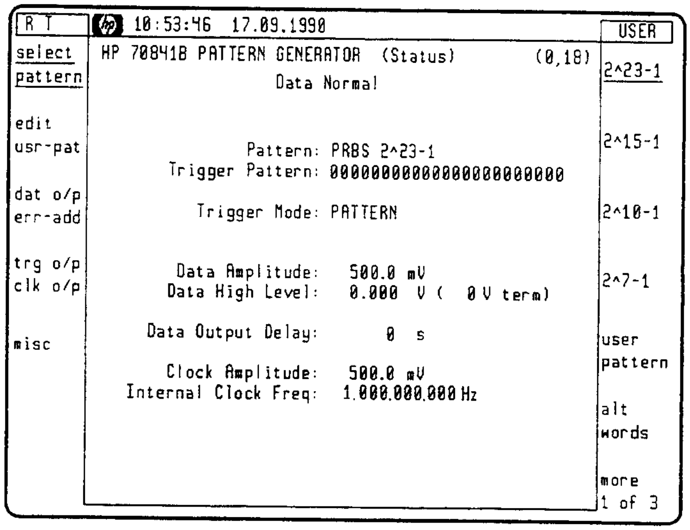


Note All unused Pattern Generator ports must be terminated in 50Ω

The HP 15680A RF Accessory Kit contains the 50Ω terminations

2. Switch on the two *Line* power switches (in any order) - wait approximately 15 seconds for selftest to end.

3. Press the Display (INST PRESET) key to set up the instrument preset parameters. The display should be as follows:



4. Check that the displayed clock frequency is 1 GHz and that the module *ACT* indicator is lit.

5. Press the Display (DISPLAY) key, the module *ACT* indicator should extinguish and an *A* should appear at the top left of the display.

6. Press the Display (MENU) key, the *A* should disappear and the *ACT* indicator should light.

7. Set the Frequency Counter Scale to Ratio B/A.

8. Check that the reading on Frequency Counter is 34217712.0. The Frequency Counter sensitivity may require adjustment to obtain a stable reading.

9. Set the Frequency Counter to Ratio C/A.

10. Press 2^7-1 .

11. Check that the reading on the Frequency Counter is 16256.0 ±0.1. The Frequency Counter sensitivity may require adjustment to obtain a stable reading.

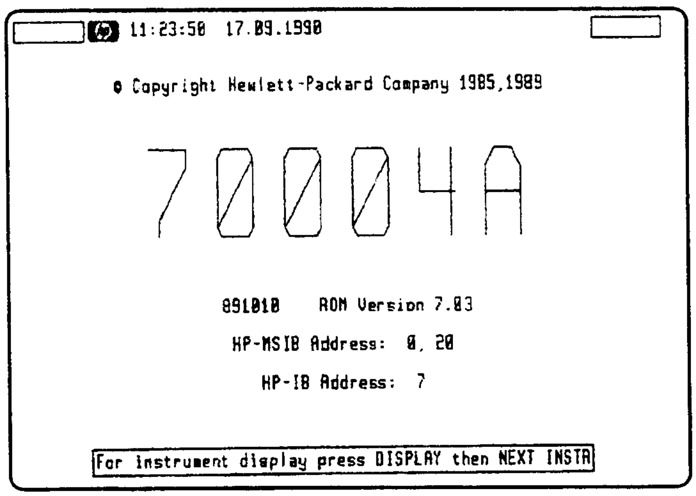
If the system does not operate as described (ie, selftest fails or error indicators are lit after selftest), go to the troubleshooting in chapter 5.

If there are no errors, the system is ready for use.

Selftest at Power-on

At power on the Error Performance Analyzer system or Pattern Generator system performs a selftest (this takes approximately 15 seconds to complete), during this time the Display, Mainframe, Error Detector and Pattern Generator modules and Clock Source operate as follows:

Display The display is blank for the first few seconds of the selftest, it then shows a multi-colored raster. The raster sweeps to the right, to show a blue back-ground. For the remainder of the selftest the display is as follows:



After selftest the Display may continue to display the above, or will display the module parameters present prior to the last power down.

Mainframe All front panel indicators extinguish except for *LINE*.

Error Detector Module All front panel indicators are lit for approximately eight seconds then extinguished for the remainder of the selftest.

After selftest the *ACT* indicator should light.

Pattern Generator Module All front panel indicators are lit for approximately five seconds then extinguished for the remainder of the selftest.

After selftest the *ACT* indicator should light.

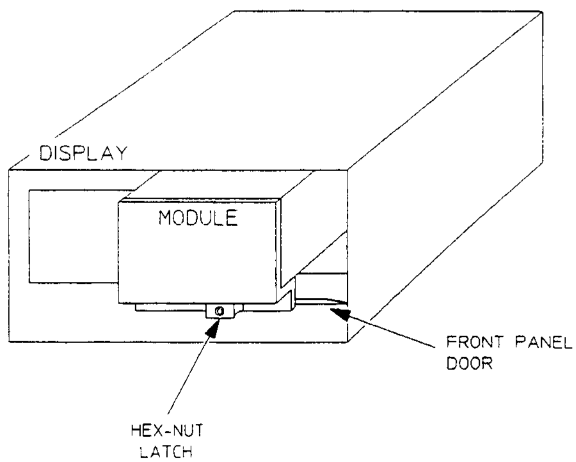
Clock Source Module All front panel indicators are lit for approximately five seconds then extinguished for the remainder of the selftest.

After selftest the *ACT* indicator should light.

Installing/Removing Modules

Use the following procedures to install your module into the Display or Mainframe. To remove a module, perform the steps in the reverse order.

Installing a Module into a Display

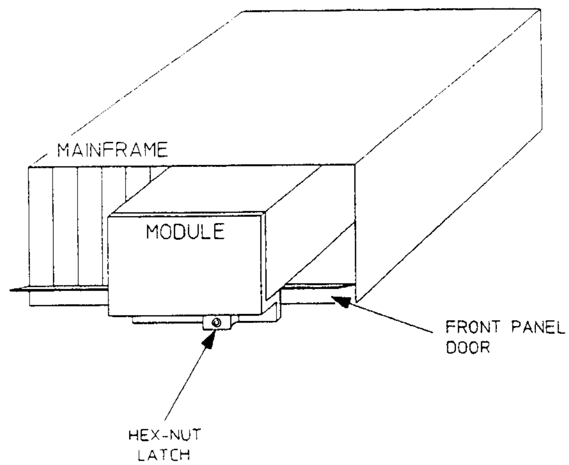


1. Open the front panel door then insert the module.
2. Secure the module by pressing against its front panel while tightening the hex-nut latch with an 8 mm hex-ball driver.

When removing an Error Detector module, disconnect any cable that may be connected to the rear panel *ERROR OUT* port.

When removing a Pattern Generator module, disconnect any cable that may be connected to the rear panel *AUX IN* port.

Installing a Module into a Mainframe



1. Open the front panel door, then insert the Clock Source module into the right side of the Mainframe.

Caution The Mainframe LINE power switch must be set to off before the front panel door will open.

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2. Secure the module by pressing against its front panel while tightening the hex-nut latch with an 8 mm hex-ball driver.
3. Insert the Pattern Generator module into the left side of the Mainframe.
4. Secure the module by pressing against its front panel while tightening the hex-nut latch with an 8 mm hex-ball driver.

When removing a Pattern Generator module, disconnect any cable that may be connected to the rear panel *AUX IN* port.

3

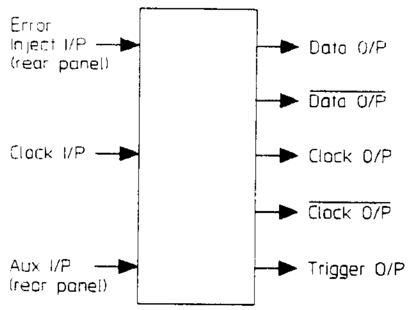
Specification

Introduction

Except where otherwise stated, the following parameters are the warranted performance specifications. Parameters described as *typical* or *nominal* are supplemental characteristics which provide a useful indication of typical, but non-warranted, performance characteristics. All specifications are for 0°C to 45°C after 30 minutes.

Pattern Generator Module

The HP 70841B is a pattern generator module in Hewlett-Packard's Modular Measurement Systems (MMS). It occupies 4/8 module slots and has eight I/O ports, six on the front panel and two on the rear:



Operating Frequency Range:
100 Mb/s to 3 Gb/s.

Patterns

PRBS Test Patterns:
2^{31}-1, polynomial D31 + D28 + 1=0, inverted.
2^{23}-1, polynomial D31 + D28 + 1=0, inverted (as in CCITT Rec 0.151).
2^{15}-1, polynomial D15 + D14 + 1=0, inverted (as in CCITT Rec 0.151).
2^{10}-1, polynomial D10 + D7 + 1=0, inverted.
2^{7}-1, polynomial D7 + D6 + 1=0, inverted.
Zero Substitution/Variable Mark Density Test Patterns:
8192 bits, based on 2^{13}-1 PRBS;
2048 bits, based on 2^{11}-1 PRBS;
1024 bits, based on 2^{7}-1 PRBS.
Zero Substitution: Zeros can be substituted for data to extend the longest run of zeros in the above patterns. The longest run can be extended to the pattern length, minus one. The bit after the substituted zeros is set to 1.
Variable Mark Density: The ratio of 1s to total bits in the above patterns can be set to 1/8, 1/4, 1/2, 3/4 and 7/8.
User programmable test patterns:
Variable length user patterns from 1 to 4,194,304 bits.
Resolution:
1 bit to 32,768 bits in 1 bit steps
32,768 to 65,536 bits in 2 bit steps
65,536 to 131,072 bits in 4 bit steps
131,072 to 262,144 bits in 8 bit steps
262,144 to 524,288 bits in 16 bit steps
524,288 to 1,048,576 bits in 32 bit steps
1,048,576 to 2,097,152 bits in 64 bit steps
2,097,152 to 4,194,304 bits in 128 bit steps

Alternating Test Patterns: Alternate between two equal length user-programmable patterns, each up to 2,097,152 bits long, under the control of a front panel key or the auxiliary input; changeover is synchronous with the end of a word. The length of the alternating word patterns should be a multiple of 128 bits.

User-programmable pattern load/save: User programmed patterns can be stored in four internal pattern stores or on a built-in 3.5 inch floppy disc. Each internal store can hold one pattern up to 8192 bits long.

Floppy disc:
Type: 3.5 inch floppy.
File format: MS-DOS
Capacity: up to 8 user programmable patterns, 1.44 Mbytes formatted.

Error Add: There are three modes of operation:
Single errors on demand;
Fixed error ratios of 1 error in 10^n bits, n=3, 4, 5, 6, 7, 8, 9.
External: Injects a single error in the transmitted test pattern on each rising edge on the error inject input.

Clock Input

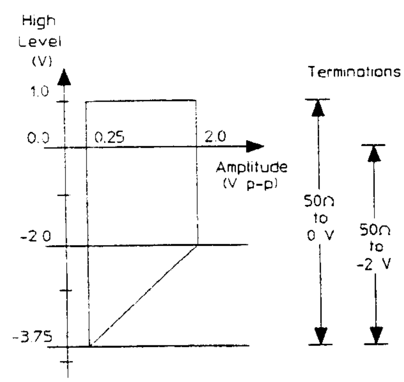
Waveform: Sinewave from the HP 70311A 3.3 GHz clock source module.
Amplitude Range: 4 dBm.
Return Loss: Over operating frequency range: > 10 dB typical.
Impedance: 50 Ω nominal.
Interface: ac coupled.
Connector: N-type female.

Alternative Clock Sources: The HP8665A, HP 8664A and 8644A synthesized signal generators are compatible. Other clock sources can be used provided they meet the following criteria:
Noise: SSB broadband noise floor, offsets > 10 MHz from the carrier in the range 10 MHz to 4 GHz:

Carrier Frequency	Noise Floor in dBc/Hz
< 300 MHz	< - 140
300 MHz to 1.0 GHz	< - 130
1.0 GHz to 2.0 GHz	< - 130
> 2.0 GHz	< - 140

Data and $\overline{\text{Data}}$ Outputs

Except where stated, all specifications are with the outputs terminated 50Ω to 0 V. The data outputs can be set to zero volts by a front panel switch.
Data Polarity: Nominal or inverted.
Format: NRZ.
Levels: Selectable amplitude and offset or nominal ECL, into 50Ω to 0 V or 50Ω to -2 V.
Amplitude:
Range: 0.25 to 2 V p-p nominal.
Resolution: 10 mV nominal.
Offset: The output amplitude and offset (high level) can be set as shown below:



High Level Resolution: 10 mV nominal.

ECL:
High Level: -0.90 V nominal.
Low Level: -1.75 V nominal.
Delay: Data delay variation vs clock output transitions:
Range: 1 ns nominal.
Resolution: 10 mV nominal.
Jitter: Specified for 2^{23}-1 PRBS, 2 V p-p output amplitude, 0 V high level and measured relative to clock: < 10 ps rms (typical jitter less than 5 ps rms).
Transition Times and Overshoot:
Specified for 3 GHz frequency 0101 pattern, 1 V p-p output amplitude and 0 V high level at 25°C.
Transition Times:
10% to 90% < 120 ps (typical).
Specified over full operating frequency range for 0101 patterns, 0.5 to 2V p-p output amplitude and 0 V high level.
Transition Times (typical):
10% to 90% < 150 ps < 300 ps
Preshoot/Overshoot: < 15% typical.
Impedance: 50Ω nominal.
Interface: dc coupled.
Connectors: N-type female.

Clock and $\overline{\text{Clock}}$ Outputs

All specifications are for the output terminated 50Ω to 0 V.
Levels: Selectable amplitude and offset or nominal ECL, into 50Ω to 0 V or 50Ω to -2 V.
Offset: The output amplitude and offset (high level) can be set as shown in the diagram in Data and $\overline{\text{Data}}$ Outputs.
Amplitude:
Range: 0.5 to 2 V p-p nominal.
Resolution: 10 mV nominal.
High Level Resolution: 10 mV nominal.
ECL:
High Level: -0.90 V nominal.
Low Level: -1.75 V nominal.
Transition Times and Overshoot:
Transition Times: 10% to 90% at 25°C (typical).

3 GHz	< 120 ps
1 GHz	< 130 ps
100 MHz	< 1.3 ns

Preshoot/Overshoot: < 15% typical at 25°C.
Impedance: 50Ω nominal.
Interface: dc coupled.
Connectors: N-type female.

Trigger Output

Provides a trigger pulse synchronous with the pattern or clock. There are two modes of operation: pattern mode and clock/32 mode.
Pattern Mode: For all patterns except alternate word, the output is a 16-clock-period trigger pulse synchonized to repetitions of the pattern. The pulse repetition rate depends on the pattern length (with the exception of alternate word patterns) and occurs at least every 128 repetitions of the pattern. The rising edge of the trigger pulse is active.
PRBS Test Patterns (2^n-1): Pulse synchronized to a selectable trigger pattern n-bits long in the PRBS.
Word Test Patterns: The trigger pulse can be synchronized to any bit in the pattern.
Alternate Word Test Patterns: Trigger output changes as the word alternates under control of the auxiliary input.
Clock/32 Mode: The trigger pulse output is the input clock divided by 32.
Pulse Amplitude: Output terminated 50Ω to 0 V.
High: 0 V nominal.
Low: -0.75 V nominal.
Impedance: 50Ω nominal.
Interface: dc coupled.
Connectors: N-type female.

Auxiliary Input

Provides a means of controlling the alternate user programmable test pattern changeover or forcing the data output to a fixed high level.

Alternate Word Selected: The input signal forces a change between the two user programmable test patterns (A and B) at the end of either pattern. The input controls which pattern is transmitted in one of two modes:
Oneshot: A single B pattern is inserted in repetitions of A pattern on a rising edge on the auxiliary input.
Alternating: The logic state on the auxiliary input determines which pattern is transmitted. Pattern A is transmitted when the logic state is "0".
Alternate Word Not Selected:
The input signal forces the data output to a fixed high level.
Levels: TTL compatible, active low.
Pulse Width:

Clock Rate	Minimum Pulse Width
> 500 MHz < 500 MHz	100 ns 250 ns

Interface: dc coupled.
Connector: BNC female.

Error Inject Input

Connector: BNC female
Levels: TTL compatible
Minimum Pulse Width:

Clock Rate	Minimum Pulse Width
500 MHz < 500 MHz	100 ns 250 ns

Data Polarity: Selectable normal or inverted data.

Frequency Measurement

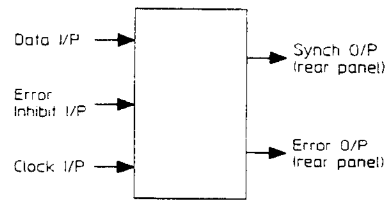
Measures the incoming clock frequency to five significant digits.

Status Indicators

Front Panel LEDs:
Clock Loss: Indicates nominal low clock power or overload at Clock Input.
HP-IB and HP-MSIB: Six LEDs indicate status.

Error Detector Module

The HP 70842B error detector module complements the HP 70841B pattern generator module. It occupies 4/8 MMS module slots and has five I/O ports, two on the front panel and three on the rear.



Operating Frequency Range:
100 Mb/s to 3 Gb/s.
To avoid duplication, reference will be made to the pattern generator section where appropriate.

Patterns

PRBS, with or without zero substitution/ variable mark density, and user programmable test patterns are as specified for pattern generator modules. For alternating user test patterns, the "A" pattern is the reference pattern.
Data Polarity: Selectable normal or inverted data.

Clock Input

Waveform: Compatible with the output of the following:
Clock Source Modules: HP 70311A.
Signal Generators: HP 8665A, 8664A.
Pattern Generator Modules: HP 70841A, 70841B.
Amplitude Range: 4 dBm.
Return Loss: Over operating frequency range: > 10 dB typical.
Impedance: 50Ω nominal.
Interface: dc coupled.
Input Termination: switchable 0 V or 2 V.
Connectors: N-type female.
Alternative Clock Sources: Other clock sources offering a similar performance to those listed under Waveform above can be used provided they meet the following criteria:
Noise: SSB broadband noise floor, offsets > 10 MHz from the carrier in the range 10 MHz to 4 GHz:

Carrier Frequency	Noise Floor
< 300 MHz > 300 MHz	< -140 dBc/Hz < -130 dBc/Hz

Data Input

Data Sampling Clock Edge: Selectable rising or falling edge.
Termination Voltage: Selectable 0 V or -2 V nominal.
Levels: Amplitude: Min, 0.5 V p-p nominal, typically better than 50 mV with 2^{23}-1 PRBS at 2.5 Gb/s;
Max, 2.0 V p-p nominal. Offset (nominal):

	Terminations	
	50 Ω to 0 V	**50 Ω to -2 V**
Maximum Input Voltage	+1 V	0 V
Minimum Input Voltage	-4 V	-4 V

0/1 Threshold: The electrical interface allows for a range of input amplitudes and dc offsets. The 0/1 threshold is set using one of three modes:
Automatic Track: Tracks the mean dc level of the input signal. The measured threshold is displayed.
Automatic Center: The error detector sets the 0/1 threshold midway between two points, top and bottom of the "eye", where the bit error ratio is equal to a selectable threshold. The "eye" height is calculated and displayed.
Manual: Sets the 0/1 threshold manually.
Range: +1 to -3 V nominal.
Resolution: 1 mV nominal.

Delay:
The data sampling point can be set automatically to the center of the "eye". The error detector sets the data/clock delay midway between two points either side of the "eye" where the bit error ratio is equal to a selectable threshold. The "eye" width is calculated and displayed. The sampling point can also be set manually by altering the data/clock delay.

Data delay variation vs selected clock edge:
Range: 1 ns nominal.
Resolution: 1 ps nominal.
Automatic Data/Clock Alignment and 0/1 Threshold Center: Selectable error-ratio thresholds from 1×10^{-7} to 1×10^{-1}.
Return Loss: 300 kHz to 3 GHz: > 10 dB typical.
Impedance: 50Ω nominal.
Interface: dc coupled.
Connectors: N-type female.

Error Output

Provides an electrical signal to indicate received errors. The error output pulse is the logical "OR" of all errors in a 16-bit period.

All specifications are for the output terminated 50Ω to 0 V.

Format: RZ, active high.
Amplitude:
High: 0 V nominal.
Low: -1.1 V nominal.
Pulse Width: For 1-bit error: 16 clock periods nominal.
Impedance: 50Ω nominal.
Interface: dc coupled.
Connector: BNC female.

Error Inhibit Input

Inhibits the counting of errors. Counting is inhibited for multiples of 16 clock periods.
Levels: ECL terminated to -2 V 50Ω, active high.
Pulse Width:

Clock Rate	**Minimum Pulse Width**
> 500 MHz	100 ns
< 500 MHz	250 ns

Connector: BNC female.

Pattern Trigger Output

Provides a pulse synchronous with the error detector reference pattern.
Format: Active high.
Amplitude:
High: 0 V nominal.
Low: -1.1 V nominal.
Pulse Width: 16 clock periods nominal.
Impedance: 50Ω.
Interface: dc coupled.
Connector: BNC female.

Audible Error Indicator

There is a selectable, audible beep on error. Single errors produce a beep. For error ratios above 1×10^{-9}, beep repetition rate increases with error ratio in five steps: 1×10^{-9}, 10^{-7}, 10^{-5}, 10^{-3}, 10^{-1}.
Requires an MMS display.

Measurement Period

Length: The length of the measurement period can be set as a time period, number of bits or number of errors.
Timed Measurement Period: Can be set from 1 second to 99 days 23 hours 59 minutes 59 seconds in 1 second steps.
Number of Bits: The time for the number of bits to be received to a resolution of 1 second. Can be set for 10^n bits, n=7, 8, 9, 10, 11, 12, 13, 14, 15.
Number of Errors: Time for number of errors to be detected to a resolution of 1 second. Can be set for 10, 100 or 1000 errors.
Real-time Clock: Provides time and date information for event logging. Battery back-up allows clock to continue running when the instrument is switched off or power fails.
Elapsed Time Indication: Shows elapsed time from the start of a gating period; resets to zero at the start of each gating period; holds value when measurement stopped.
Gating Periods: There are three gating (measurement timing) modes: Manual, Timed Single and Timed Repeat.
Manual: Gating period is controlled by the Run/Stop Gating keys. Accumulating results are displayed throughout the measurement and the end of measurement results are held until a new gating period is started.
Single: Gating period is started by pressing the Run Gating key and terminates at the end of the gating period set by the user. Accumulating results are displayed throughout the gating period and the end of gating results are held until a new gating period is started.
Repeated: Similar to Single but when one timed gating period ends, a new dentical period starts. This continues until the measurement is terminated by pressing the Stop Gating key. The measurement results displayed during any period can be the final results of the previous period or the accumulating results for the current period. There is no "deadtime" betwen consecutive periods. The gating period excludes any periods when the instrument is not powered.

Error Measurements

The error detector counts bit errors by comparing the incoming data bit-by-bit with the internally-generated reference pattern. Error count and ratio are calculated for three types of errors, errored ones, errored zeros and all logic errors. All measurements run during the gating periods as described with the exception of Delta Error Count and Delta Error Ratio. These measurements run continuously to facilitate user adjustments for minimizing errors.
Error Count: The total number of error ones, zeros and all logic errors during the gating period.
Delta Error Count: The number of logic errors in successive decisecond intervals.
Error Ratio: The ratio of counted errored ones, errored zeros and all logic errors to the number of bits in the selected gating period.
Delta Error Ratio: The ratio of counted logic errors to the number of bits in successive decisecond intervals.
Errored Intervals: Time intervals during which one or more errors occurred. These intervals are errored seconds, deciseconds, centiseconds or milliseconds.
Error Free Intervals: Time intervals of seconds, deciseconds, centiseconds or milliseconds, during which no errors occurred.

Error Analysis

The error analysis is based on CCITT Rec G.821 and is derived from the bit error results.
%Unavailability: The error ratio is calculated over 1 second timed intervals during the gating period. An unavailable period begins when the error ratio is worse than 1×10^{-3} for 10 consecutive seconds. These 10 seconds are considered part of the unavailable time.
The unavailable period ends when the error ratio is better than 1×10^{-3} for 10 consecutive seconds. These 10 seconds are considered part of the unavailable time. %Unavailability is the ratio of the unavailable seconds to the total gating period expressed as a percentage.
%Availability: The ratio of the available seconds to the total gating period expressed as a percentage.
%Errored Seconds: The ratio of the errored seconds in the available time to the total number of seconds in the available time, expressed as a percentage.
%Severely Errored Seconds: The ratio of the total number of available seconds with an error ratio worse than 1×10^{-3} to the total number of available seconds, expressed as a percentage.
%Degraded Minutes: Severely errored seconds are discarded from the available time and the remaining seconds are grouped into blocks of 60 seconds. Blocks which have an error ratio worse than 1×10^{-6} are called degraded minutes and % degraded minutes is the ratio of the total

number of degraded minutes to the total number of 60 second blocks in the available time expressed as a percentage.

Power-loss Seconds

Displayed as the number of seconds the error detector is not able to make measurements during a gating period owing to ac-power-loss. The gating continues to the end of the selected period following restoration of power.

Sync-loss Seconds

Displayed as the number of seconds the error detector loses pattern synchronisation during a gating period.

Pattern Synchronisation

Synchronisation to the incoming pattern can be performed automatically or manually. In manual mode, the Sync Start key forces the error detector to attempt synchronisation with the received pattern.
Sync Gain/Loss Criteria: The criteria for gaining or losing synchronisation is the error ratio in a 1 ms interval. Selectable error-ratio thresholds of 1×10^{-1}, 10^{-2}, 10^{-3} or 10^{-4} are provided.
Resync Time:
PRBS 2^{31}-1, 2^{23}-1, 2^{15}-1, 2^{10}-1: < 200 ms nominal;
PRBS 2^{10}-1, 2^{7}-1: < 500 ms nominal.
Word patterns: Dependent on pattern length and autocorrelation properties of pattern. Example: STM16 frame and PRBS data at 2.5 Gb/s have resync time less than 5 seconds.

Frequency Measurement

The incoming clock frequency is measured and displayed to five significant digits.

Result Logging

Results can be logged to most standard HP-IB 80-column printers. There are two modes of operation: with and without an external controller.

With an external controller, information on results, status and alarms is provided for the controller.

Without an external controller, the error detector module can be set to controller mode to permit output of results, status and alarms to an external printer or other logging device.

Print Modes: Two modes are provided:
On-Demand: Prints time-of-day and selected set of results when Log On Demand key is pressed.
Gating: logs time-stamped events during gating and/or a user-selected summary of measured results and alarm durations at the end of each gating period. A conditional printing trigger can be set so that printing occurs only on errors or error ratios exceeding a value selected by the user.

Status Indicators

Front Panel LEDs:
Gating: Signifies measurements in progress.
Clock Loss: Indicates nominal low clock power at Clock Input.
Data Loss: Indicates no transitions in the last decisecond.
Sync Loss: Illuminated in accordance with sync gain/loss criteria as specified.
Errors: Indicates one or more data errors in the last decisecond.
HP-IB/MSIB: Six LEDs indicate status.

Clock Source Modules

The HP 70311A is a clock source module in Hewlett-Packard's Modular Measurement System. It occupies 4/8 module slots and has a clock output and an external reference input. It provides a variable synthesized clock signal to the pattern generator.

Frequency:
Range: 16 MHz to 3.3 GHz
Resolution: 1 Hz
Stability:
ageing 2 ppm/year after 1 year,
temperature 6 ppm over 0 to 45°C.

Spectral purity:
Harmonics: < -30 dBc.
SSB phase noise on 3.3 GHz carrier at 1 kHz offset is -75 dBc/hz and at 20 kHz offset is -115 dBc/Hz.
Output Level: Fixed in the range 3 dBm.
Connector: N-type female, 50Ω, ac coupled.

External reference input:
Connector: SMB male, rear panel
Input Impedance: 50Ω, ac coupled.
Frequency: 10 MHz 1 kHz.
Amplitude: 230 mV rms to 2 V rms.
Note: The HP 70311A clock source does not have AM or FM modulation capability.

General

Remote Control

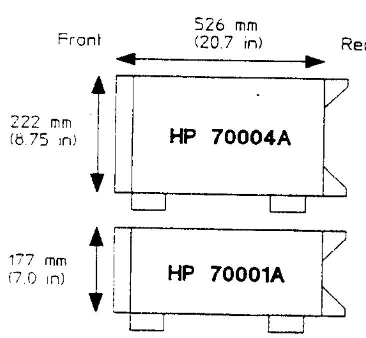
HP-IB Interface and Capability:
Operates according to IEEE standard 488.1 and 488.2, 1987. Conforms, where appropriate, to the Standards Commands for Programmable Instruments (SCPI) standard 1990.0.
Capability: SH1, AH1, T6, TE0, L4, LE0, SR1, RL1, PP0, DC1, DT0, C1, C2, C3, C28.
Modes: Addressable or controller.
Addressable: An external controller has access to all the current results, status and alarms and can control all module functions except HP-IB, HP-MSIB addresses and power switch.
Controller: The HP 70842B error detector module outputs results to an external printer over HP-IB without an external controller.

Power Requirements

Voltage Range: Selectable 100, 120, 220 and 240 V ac (10%) nominal.
Frequency Range: 44 to 66 Hz and 400 Hz nominal.
Power Consumption:
HP 71603B: 1000 VA max.
HP 71604B: 800 VA max.
All module power requirements are supplied by the mainframe or display.

Physical

Dimensions:
Width: all units: 425 mm (16.75 in).
Height and Depth: See sideview diagram below.



Add 23 mm (0.91 in) to depth to include front panel connectors.

Weight (nominal):
HP 71603B error performance analyzer: 60 kg (130 lb) net.
HP 71604B pattern generator: 54 kg (117 lb) net.
Elements:
HP 70001A mainframe: 14.5 kg (32.0 lb) net.
HP 70004A display: 20.0 kg (44 lb) net.
Plug-in Modules: HP 70311A signal generator: 8.9 kg (20 lb) net.
HP 70841B pattern generator: 6.5 kg (14 lb) net.
HP 70842B error detector: 6.0 kg (13 lb) net.

Environmental

Operating Temperature Range:
0°C to 45°C.
Storage Temperature Range:
-40°C to +65°C.
Humidity: Operation 15% to 95% relative humidity at 40°C, non-condensing.
EMC: Conducted and Radiated interference is in compliance with CISPR Pub 11, FTZ 526/1979, and MIL-STD 461B RE02/part 7.
Calibration Interval: Recommended one year.

4

Performance Tests

Introduction

Module Verification

This chapter contains procedures to test the electrical performance of the Pattern Generator and Error Detector modules to the specifications listed in chapter 3.

The Pattern Generator module test procedures start on page 4-4.

The Error Detector module test procedures start on page 4-51.

System Verification

If the electrical performance of an Error Performance Analyzer or Pattern Generator system has to be verified, then in addition to the above tests each element in the system must be checked, using the performance tests from the appropriate manual.

Use the following table to identify the elements (by product number) which make up the system to be tested.

Element	HP 71603B Error Performance Analyzer	HP 71604B Pattern Generator
Display *	HP 70004A	HP 70004A
Mainframe	HP 70001A	HP 70001A
Pattern Generator	HP 70841B	HP 70841B
Error Detector	HP 70842B	-
Clock Source	HP 70311A	HP 70311A

*Monochrome Display HP 70205A or HP 70206A may be substituted.

Test Levels

There are two levels of performance testing:

Operational Verification — Provides >90% confidence that the system or module is operating to its full warranted specification.

Full Performance Test — Ensures that the system or module is operating to its full warranted specification.

Performance tests for the Pattern Generator and Error Detector must be done in the order shown. A list of the recommended test equipment required is given in the table on page 4-3.

Results of each module Performance Test may be recorded on the Test Record at the end of chapter 4, or on the Abbreviated Test Record for Operational Verification.

If any module test fails to meet specification, refer to the Adjustments in the *Service Manual*. If after adjustment the specification still cannot be met, refer to the *Troubleshooting* in Chapter 5 of this manual.

Calibration Cycle

The system requires periodic verification of performance. Results may be recorded on the Test Record at incoming inspection and used for comparison in yearly maintenance and calibration or after repairs or adjustments.

Warm-up Time

The system must be switched on for a minimum of 30 minutes before carrying out any tests.

Measurement Uncertainties

Performance Test Limits

All the measurements made in the performance test section of this manual comply with the 4:1 required by Mil Std 45662A. The tests involving critical specifications use a frequency counter and an oscilloscope. The uncertainties of both pieces of equipment are explained below.

Frequency Counter Measurements

All the measurements made with the frequency counter(s) are A/B ratio measurements hence timebase and trigger uncertainties can be neglected. Therefore the accuracy is the measured value, plus or minus one count.

Rise Time Measurements

There are two factors to be taken into consideration here, the rise time of the oscilloscope and the rise time of the cables. The cables used are the ones supplied in the HP 15680A Accessory Kit. These cables are specified to have an effective bandwidth of 40 GHz.

The cable rise time is = 0.35/40 = 8.75 ps.
The specified rise time of the HP 54121T Oscilloscope is 19.4 ps.
The maximum rise time of the measuring system is derived from the calculations below.

$$\sqrt{8.75^2 + 19.4^2} = 22ps$$

In all cases this exceeds the 4:1 requirement.

Recommended Test Equipment

The test equipment required is listed in the following table. Equipment which meets or exceeds the critical specifications may be substituted for the recommended model.

Recommended Test Equipment

Instrument	Critical Specification	Recommended Model	Use *
Display Unit **	Unique	HP 70004A	PATO
Mainframe Unit **	Unique	HP 70001A	PATO
Pattern Generator **	Unique	HP 70841A/B	PATO
Digitizing Oscilloscope	> 20 GHz Bandwidth	HP 54121T	PATO
Four Channel Test Set	50 Ω Termination. Interface to Digitizing Oscilloscope with selectable attenuation.	HP 54121A	PATO
Frequency Counter	Frequency Range 10 Hz-1.3 GHz, Ratio Measurement.	HP 5328B Opt 031	PTO
Microwave Counter	Frequency Range 10 Hz-3 GHz	HP 5343A; HP 5342A	PTO
Pulse Generator	12 MHz to 5 MHz pulse rate; Variable pulse width 100 to 250 ns; Amplitude ≥5 Vpk-pk.	HP 8116A	PATO
Synthesized Sweeper	50 MHz-3 GHz Sinewave RF. Output −10 to +10 dBm. Noise < −140 dBc, f < 300 MHz; < −130 dBc, 300 MHz-2 GHz; < −140 dBc, f > 2 GHz.	HP 83620A; HP 8665A	
Pulse Generator	1 to 5 MHz pulse; Variable width 0 to 100%	HP 8116A	PTO
RF Accessory Kit	Cables and connectors supplied with unit.	HP 15680A	PATO
Power Meter	−10 to +10 dBm ±0.03 dB; 50 MHz to 3 GHz.	HP 436A	PATO
Power Sensor	−10 to +10 dBm ±2%; 50 MHz to 3 GHz; 50Ω.	HP 8481A; HP 8482A	PATO
Power Splitter	Output Tracking <0.1 dB; 50 MHz to 3 GHz; 50Ω.	HP 11667A; HP 11667B	PATO
Attenuator (fixed 10 dB)	50 MHz to 1 GHz; ±1 dB; 50Ω.	HP 8491A; HP 8491B	PATO

*P=Performance Tests; A=Adjustments; T=Troubleshooting; O=Operational Verification
** May be a calibrated part of the system under test.

Operational Verification

The Operational Verification tests quickly establish with >90% confidence that the HP 71600 Series meets the specifications listed in Chapter 3. The following table lists all the Operational Verification Tests.

Operational Verification

Test	Page Number
Pattern Generator Checks	
Clock Input Levels	4-6
Clock Output Waveforms	4-10
Data Output Waveforms	4-16
PRBS 2^n-1 Pattern Length	4-27
Error Detector Checks	
Clock Input Levels	4-55
PRBS 2^n Synchronization, Error Detect and Memory Backup	4-62
Error Output Waveform and Data Input Delay	4-79

Pattern Generator Performance Tests

These tests (on pages 4-6 to 4-50) ensure that the HP 70841B 0.1-3 GHz Pattern Generator module meets specification. Before carrying out any of the tests - do the *Pattern Generator Module Preliminary Setup*.

Test Frequencies

The terms *minimum* and *maximum* are used to define test frequencies in the performance tests. These frequencies are defined in the following table:

Module	Minimum Frequency	Maximum Frequency
HP 70841B	100 MHz	3 GHz

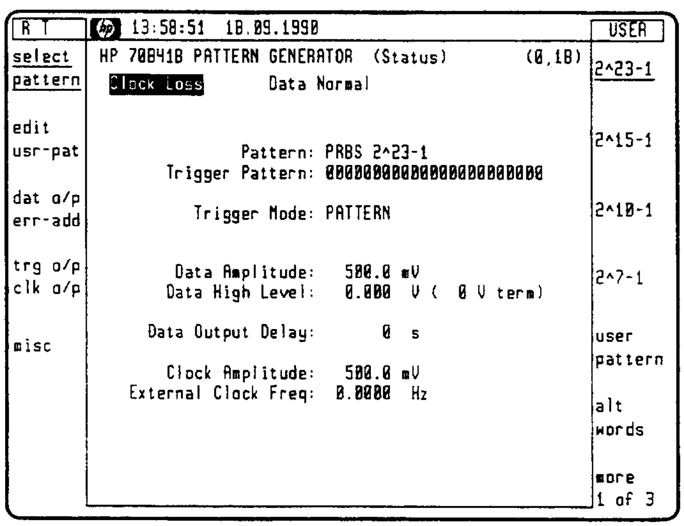
Clock Source

The HP 83620A Synthesized Sweeper or equivalent (see the *Recommended Test Equipment* on page 4-3) provides the clock signal for the Pattern Generator module in the following performance tests.

Note The system Clock Source should not be used for performance testing.

Pattern Generator Module Preliminary Setup

1. Note the Pattern Generator module HP-MSIB address (row, column). It must be returned to this setting after its performance has been verified.
2. Set the *row* address to 0 and the *column* address to 18, see page 2-8.
3. Plug the Pattern Generator module (to be tested) into the HP 70004A Display.
4. Power-on the Display (system selftest occurs at power-on, takes approximately 15 seconds to complete.
5. Press (DISPLAY) followed by NEXT INST to establish a communication link between the Pattern Generator module and the Display.
6. Press (INST PRESET) to initialize the Pattern Generator module to its preset or default state. After several seconds the display should be as follows:



Clock Input Levels

Specifications

Clock Input

Waveform: Sinewave from the HP 70311A/HP 70322A (or equivalent) Signal Generators.

Amplitude: ±4 dBm.

Return Loss: Over operating frequency range > 10 dB typical.

Impedance: 50Ω nominal.

Interface: ac coupled.

Connector: N-type female.

Alternative Clock Sources: The HP 8665A and HP 8644A Synthesized Generators are compatible. Other clock sources can be used provided they meet the following criteria:

Noise: SSB broadband noise floor, offsets > 10 MHz from the carrier in the range 10 MHz to 4 GHz:

Carrier Frequency	Noise Floor (dBc/Hz)
	HP 70841B
< 300 MHz	< −140
300 MHz to 2 GHz	< −130
> 2 GHz	< −140

Description

A clock signal at 0 dBm is applied to the Pattern Generator *CLOCK IN* port from a Synthesized Sweeper. The Synthesized Sweeper output is reduced to the minimum level specified for the Pattern Generator *CLOCK IN* port - the *CLOCK OUT* signal is checked visually on the Digitizing Oscilloscope to ensure no degradation has occurred. The Synthesized Sweeper output is then increased to the maximum level specified for the Pattern Generator *CLOCK IN* port - again the *CLOCK OUT* signal is monitored on the Digitizing Oscilloscope to ensure no degradation has occurred. The Clock Loss alarm functions on the Pattern Generator are tested by reducing the *CLOCK IN* signal level until these alarms are displayed. These tests are repeated at two other clock frequencies.

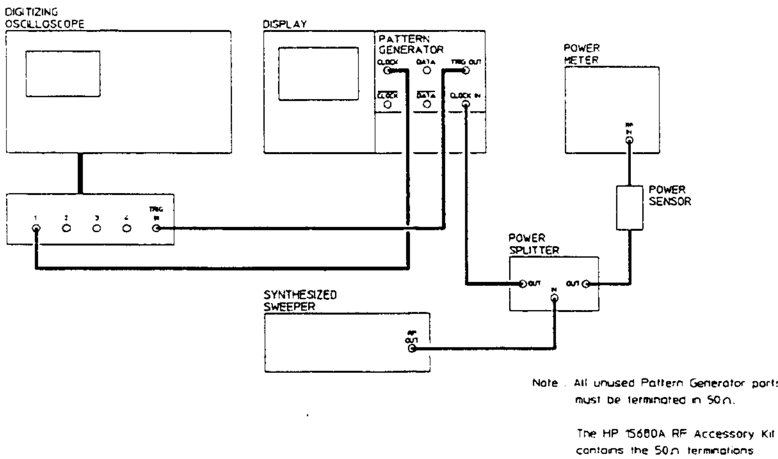
Equipment

Synthesized Sweeper	: HP 83620A
Digitizing Oscilloscope	: HP 54121T
Four Channel Test Set	: HP 54121A
RF Accessory Kit	: HP 15680A
Display	: HP 70004A
Power Meter	: HP 436A
Power Sensor	: HP 8482A
Power Splitter	: HP 11667A

Procedure

Checking the Minimum Level at the CLOCK IN port

1. Initialize the Pattern Generator, see page 4-5.
2. Press `CLK O/P` followed by **`CLOCK AMPLTD`**. Set the clock amplitude to 1 V using the numeric and **`ENTER`** keys. Set `TRIGGER PAT CLK` to `CLK`.
3. Connect the equipment as shown:



4. Set the Digitizing Oscilloscope for the following parameters:

CHAN	:	Atten X1; CH 1 on; CH 2,3,4; off CH 1 amplitude 200 mV/Div; Offset 0 mV.
TIMEBASE	:	Sweep Speed 1 ns/Div; Delay 16 ns; Delay Ref left; Triggered.
TRIGGER	:	Trig level −500 mV; Slope +ve; Atten X1; HF sense off; HF Reject off.
DISPLAY	:	Display Mode Persist; Display Time 10 s; Screen Single; Graticule grid; Bandwidth 20 GHz.

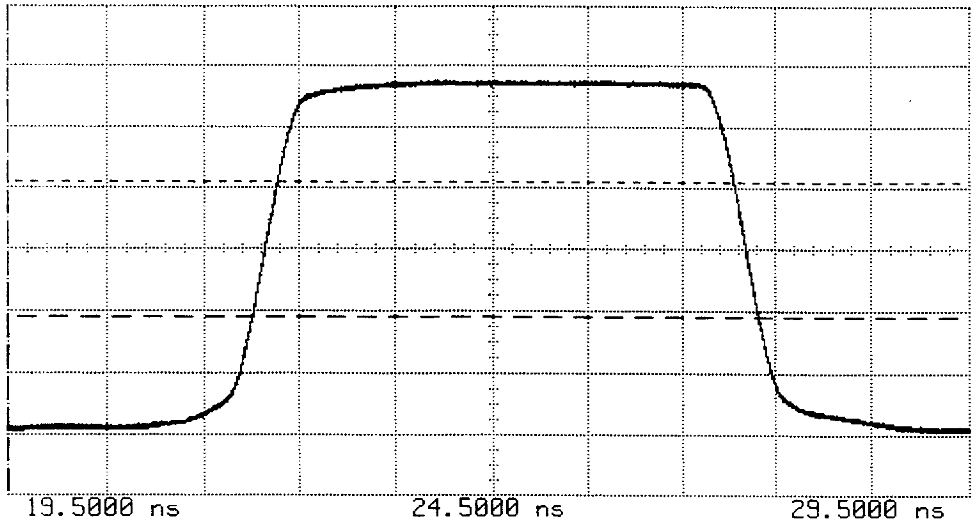
Note The above parameters may be obtained by using the Digitizing Oscilloscope *Autoscale* function and modifying as required.

5. Set the Power Meter to read *dBm* (100% CAL factor).

Note The Power Sensor should be calibrated using the Power Meter internal reference. Refer to the Power Meter Operating Manual for details.

6. Set the Synthesized Sweeper to the minimum module frequency and adjust the level for a reading of 0 dBm on the Power Meter.

7. Adjust the Digitizing Oscilloscope timebase and delay to position a single *CLOCK OUT* pulse in the center of the display. The display below shows a typical pulse for the HP 70841B module:




```
Ch. 1      =  200.0 mVolts/div        Offset    =  6.375 mVolts
Timebase   =  1.00 ns/div             Delay     =  19.5000 ns
Delta V    =  437.50 mVolts
Vmarker1   = -210.00 mVolts           Vmarker2  =  227.50 mVolts
Delta T    =  332.2   ps
Start      =  17.3120 ns              Stop      =  17.6442 ns

   Trigger on External at Pos. Edge at -480.5 mVolts
```

8. Reduce the Synthesized Sweeper for a reading of −4 dBm on the Power Meter.
9. Ensure the displayed pulse is unchanged from step 7. Any changes in pulse amplitude, risetime, falltime, preshoot and overshoot will be clearly observed on the display due to the long persist time.

Checking the Maximum Level at the CLOCK IN port

10. Increase the Synthesized Sweeper for a reading of +4 dBm on the Power Meter.
11. Ensure the displayed pulse is unchanged from step 7. Any changes in pulse amplitude, risetime, falltime, preshoot and overshoot will be clearly observed on the display due to the long persist time.

Checking Clock Loss Alarms

12. Reduce the Synthesized Sweeper level until the *CLK LOSS* alarm indicator on the Pattern Generator module is lit. The `Clock Loss` alarm message should appear on the display. Typically, *CLK LOSS* will occur below −10 dBm. Confirm this level on the Power Meter.

Checking CLOCK IN Levels at the Maximum Frequency

13. Repeat steps 7 to 12 with the Synthesized Sweeper frequency set to maximum module frequency. The Digitizing Oscilloscope timebase and delay will need to be adjusted to obtain a single *CLOCK OUT* pulse for measurement.

Clock Output Waveforms

Specifications

Clock and $\overline{\text{Clock}}$ Outputs

All specifications are for the output terminated 50Ω to 0 V.

Amplitude: Range: 0.5 V to 2 V p-p nominal. Resolution: 10 mV nominal.

Transition Times: 10 % to 90% at 25°C typical

	HP 70841B
3 GHz	< 120 ps
1 GHz	< 150 ps
100 MHz	< 1.3 ns

Preshoot/Overshoot: < 15% typical at 25°C.

Impedance: 50Ω nominal.

Interface: dc coupled.

Connectors: N-type female.

Description

A Digitizing Oscilloscope is used to measure selected parameters of the waveforms at the Pattern Generator *CLOCK OUT* and $\overline{\textit{CLOCK OUT}}$ ports and to verify *data delay*.

In the data delay test the *trigger output* signal (which is in fixed phase alignment with the *data signal*) is used as the Digitizing Oscilloscope reference and the *clock signal* position on the display indicates the data delay.

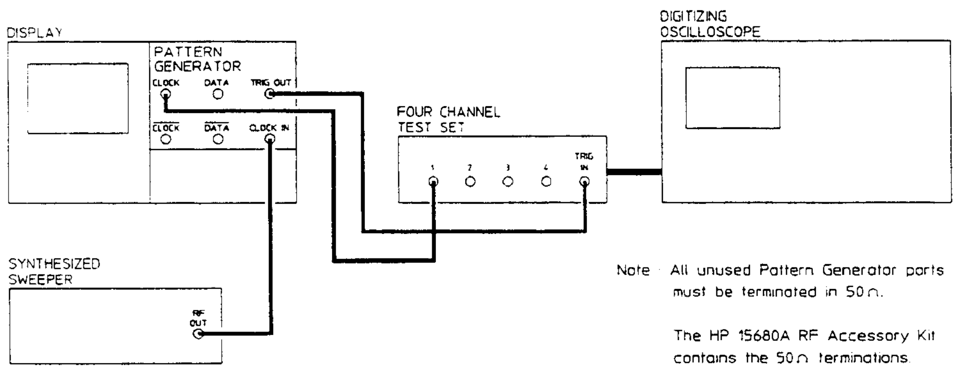
Equipment

Synthesized Sweeper	: HP 83620A
Digitizing Oscilloscope	: HP 54121T
Four Channel Test Set	: HP 54121A
RF Accessory Kit	: HP 15680A
Display	: HP 70004A

Procedure

Checking Maximum Frequency Waveforms at the CLOCK OUT Port

1. Initialize the Pattern Generator, see page 4-5.
2. Press `CLK O/P` followed by `CLOCK AMPLTD`. Set the clock amplitude to 1 V using the numeric and `ENTER` keys. Set `TRIGGER PAT CLK` to `CLK`.
3. Set the Synthesized Sweeper to the maximum module frequency and 0 dBm.
4. Connect the equipment as shown:

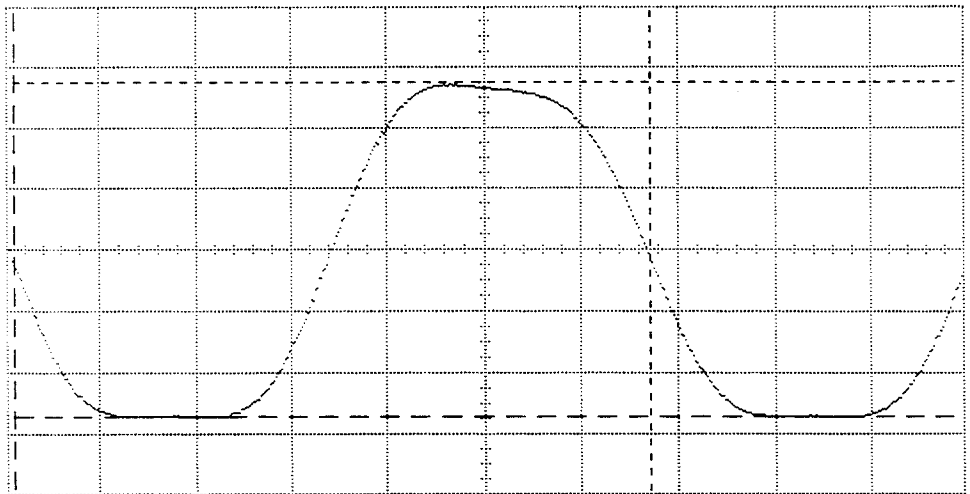


5. Set the Digitizing Oscilloscope for the following parameters:

CHAN	: Atten X3; CH 1 on; CH 2,3,4; off CH 1 amplitude 20 mV/Div; Offset 20 mV.
TIMEBASE	: Timebase 50 ps/Div; Delay 16 ns; Delay Ref left; Triggered.
TRIGGER	: Trig level −500 mV; Slope +ve; Atten X1; HF sense off; HF Reject off.
DISPLAY	: Display Mode Averaged; Number of Averages 8; Screen Single; Graticule grid; Bandwidth 20 GHz.

Note The above parameters may be obtained by using the Digitizing Oscilloscope *Autoscale* function and modifying as required.

6. Adjust the Digitizing Oscilloscope amplitude, timebase and delay to obtain a display similar to the following. The display below shows a typical waveform for the HP 70841B.



```
17.3080 ns                    17.5580 ns                    17.8080 ns

Ch. 1       =  80.00 mVolts/div            Offset      =  6.375 mVolts
Timebase    =  50.0 ps/div                 Delay       =  17.3080 ns
Ch. 1 Parameters                           P-P Volts   =  440.00 mVolts
Rise Time   =  66.4     ps                 Fall Time   =  72.4     ps
Freq.       =  3.01023 GHz                 Period      =  332.2    ps
+ Width     =  161.4    ps                 - Width     =  170.8    ps
Overshoot   =  571.4 m%                    Preshoot    =  0.000    %
RMS Volts   =  174.62 mVolts               Dutycycle   =  48.58    %

    Trigger on External at Pos. Edge at -480.5 mVolts
```

7. Use the Digitizing Oscilloscope *MEASUREMENT* function to check the following waveform parameters:

Measured Parameter	HP 70841B
Rise Time (10% to 90%)	< 120 ps
Fall Time (10% to 90%)	< 120 ps
Preshoot	< 15%
Overshoot	< 15%

Note

If poor rise and fall times are obtained, the Digitizing Oscilloscope may *NOT* be estimating the waveform 0-100% level correctly, use the following:

i. Select *Delta V* then set MARKER 1 to pulse minimum and MARKER 2 to pulse maximum using the *SET MARKER 1* and *SET MARKER 2* keys (see step 6).

ii. Set the marker preset levels to 10% and 90%.

iii. Select *Delta t*, then adjust the *Start Marker* to cross V MARKER 1 at the rising edge of the waveform.

iv. Adjust the *Stop Marker* to cross V MARKER 2 at the rising edge of the waveform.

v. Note the *Delta t* reading. This gives the waveform rise time.

vi. Select *Delta t*, then adjust the *Start Marker* to cross the V MARKER 2 at the falling edge of the waveform.

vii. Adjust the *Stop Marker* to cross the V MARKER 1 at the falling edge of the waveform.

viii. Note the *Delta t* reading. This gives the waveform fall time.

8. Repeat steps 6 and 7 with the Pattern Generator CLOCK AMPLTD set to 0.5 V and 2 V.

Checking the Maximum Module Frequency Waveforms at the CLOCK OUT Port

9. Connect Channel 1 of the Four Channel Test Set to the *CLOCK OUT* port. Ensure that the *CLOCK OUTPUT* port is terminated in 50Ω.
10. Adjust the Digitizing Oscilloscope delay to position the *one* clock pulse at the center of the display.
11. Repeat steps 6 and 7 with the Pattern Generator CLOCK AMPLTD set to 2 V, 1 V and 0.5 V.
12. Return the Pattern Generator CLOCK AMPLTD to 1 V.

Checking the Minimum Module Frequency Waveforms at the CLOCK OUT Port

13. Set the Synthesized Sweeper to the minimum module frequency and 0 dBm.
14. Adjust the Digitizing Oscilloscope amplitude, timebase and delay to obtain a display similar to that shown in step 6.
15. Use the Digitizing Oscilloscope *MEASUREMENT* function to check the following waveform parameters:

Clock Output Waveforms

Measured Parameter	HP70841B
Rise Time (10% to 90%)	< 1.3 ns
Fall Time (10% to 90%)	< 1.3 ns
Preshoot	< 15%
Overshoot	< 15%

Note

If poor rise and fall times are obtained, the Digitizing Oscilloscope may *NOT* be estimating the waveform 0-100% level correctly. Use the following manual procedure to check the rise and fall times manually on the Digitizing Oscilloscope.

i. Select *Delta V* then set MARKER 1 to pulse minimum and MARKER 2 to pulse maximum using the *SET MARKER 1* and *SET MARKER 2* keys (see step 6).

ii. Set the marker preset levels to 10% and 90%.

iii. Select *Delta t*, then adjust the *Start Marker* to cross V MARKER 1 at the rising edge of the waveform.

iv. Adjust the *Stop Marker* to cross V MARKER 2 at the rising edge of the waveform.

v. Note the *Delta t* reading. This gives the waveform rise time.

vi. Select *Delta t*, then adjust the *Start Marker* to cross the V MARKER 2 at the falling edge of the waveform.

vii. Adjust the *Stop Marker* to cross the V MARKER 1 at the falling edge of the waveform.

viii. Note the *Delta t* reading. This gives the waveform fall time.

16. Repeat steps 14 and 15 with the Pattern Generator clock output level set to 0.5 V then 2 V.
17. Return the Pattern Generator CLOCK AMPLTD to 1 V.

Checking the Minimum Module Frequency Waveforms at the CLOCK OUT Port

18. Connect Channel 1 of the Four Channel Test Set to the Pattern Generator *CLOCK OUT* port. Ensure that the $\overline{CLOCK\ OUT}$ port is terminated in 50Ω.
19. Repeat step 16.

Checking Relative CLOCK/$\overline{\text{CLOCK OUT}}$ Phases

20. Connect Channel 2 of the Four Channel Test Set to the $\overline{CLOCK\ OUT}$ port.
21. Switch on Channel 2 of the Digitizing Oscilloscope and set Channel 2 parameters to match Channel 1 (using *Autoscale* may ease setup).
22. Check that the *CLOCK OUT* and $\overline{CLOCK\ OUT}$ waveforms are 180 degrees out of phase (antiphase).

Checking Relative CLOCK/DATA OUT Phases (Data Delay Test)

23. Set the Synthesized Sweeper for a 500 MHz sinewave at 0 dBm.
24. Switch off Channel 2 of the Digitizing Oscilloscope.
25. Press `dat o/p` followed by **DAT O/P DELAY**.
26. Set the Pattern Generator **Data Out Delay** to +1 ns using the numeric keys.
27. Adjust the Digitizing Oscilloscope timebase and delay to display two clock pulses - call these LEFT and RIGHT pulses.
28. Set the Digitizing Oscilloscope display to *Persist* with a persist time of 300 ms.
29. Select *Delta V*, *Delta t* on the Digitizing Oscilloscope, then position the voltage and timing markers (ie MARKER 1 and START) to the center of the rising edge of the RIGHT pulse.
30. Slowly reduce the Pattern Generator **Data Out Delay** to −1 ns using the rotary knob. The LEFT pulse should move from left to right across the display.
31. Ensure the center of the rising edge of the LEFT pulse is now aligned with the markers.

Data Output Waveforms

Specifications

Data and $\overline{\text{Data}}$ Outputs

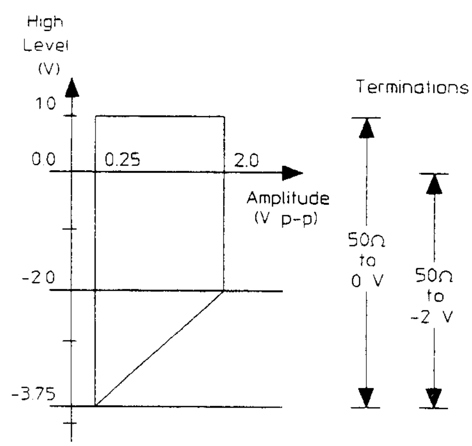
Except where stated, all specifications are with the outputs terminated 50Ω to 0 V.

Format: NRZ.

Levels: Selectable amplitude and offset or nominal ECL, into 50Ω to 0 V or 50Ω to −2 V.

Amplitude: Range: 0.25 to 2 V p-p Nominal. Resolution: 10 mV nominal.

Offset: The output amplitude and offset (high level) can be set as shown below:



High Level Resolution: 10 mV nominal.

ECL: High level: −0.90 V. Low Level: −1.75 V nominal.

Delay: Data delay variation vs clock output transition:

Range: ±1 ns nominal. Resolution: 1 ps nominal.

Transition Times: Specified for the transition highlighted in the following test pattern with 1 V p-p output amplitude and 0 V high level 25°C 0101010100000000011111111100110011
Transition Times:

	HP 70841B at 3 GHz	HP 70841B at 300 MHz
10% to 90%	< 120 ps	<150 ps
20% to 80%	< 90 ps	-

Specified over full operating frequency range for the same pattern, 0.5 to 2 V p-p output amplitude and 0 V high level.
Transition Times (typical):

	HP 70841B
10% to 90%	< 150 ps

Preshoot/Overshoot (300 MHz only): <15%

Preshoot/Overshoot (over full frequency range): < 15% typical.

Impedance: 50Ω nominal.

Interface: dc coupled.

Connectors: N-type female.

Data Polarity: Selectable normal or inverted data.

Description

A Digitizing Oscilloscope is used to measure selected parameters of the waveforms at the Pattern Generator *DATA OUT* and $\overline{DATA\ OUT}$ ports. Two spot frequencies are checked with patterns selected to optimize measurement accuracy.

Equipment

Synthesized Sweeper	: HP 83620A
Digitizing Oscilloscope	: HP 54121T
Four Channel Test Set	: HP 54121A
RF Accessory Kit	: HP 15680A
Display	: HP 70004A

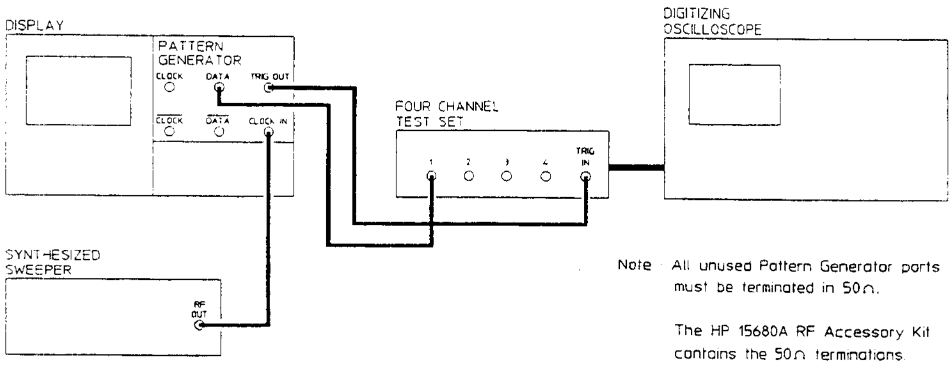
Procedure

Checking the Maximum Module Frequency Waveforms at the DATA OUT Port

1. Initialize the Pattern Generator, see page 4-5.
2. Press `dat o/p` followed by `DATA AMPLTD`. Set the data amplitude to 1 V using he numeric keys.
3. Press `DATA HI-LEVEL`. Set the data Hi level (pulse top) to 0 V using the numeric keys.
4. Press `edit usr-pat` followed by `INTERNL PATT 1`. Set the pattern to 0101 0101 0000 0000 1111 1111 0011 0011 (see *Appendix B*).
5. Press `select pattern` followed by `user pattern`. Press `user pattern` then select `INTERNL PATT 1`.
6. Set the Synthesized Sweeper to the maximum module frequency and 0 dBm.

Data Output Waveforms

7. Connect the equipment as shown:



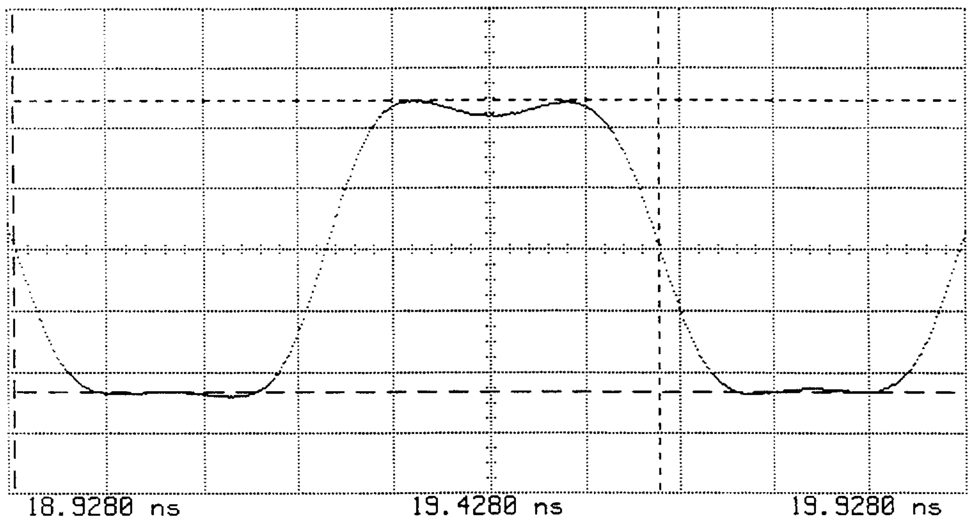
8. Set the Digitizing Oscilloscope for the following parameters:

CHAN	: Atten X1; CH 1 on; CH 2,3,4 off; CH 1 amplitude 20 mV/Div; Offset 20 mV.
TIMEBASE	: Timebase 100 ps/Div; Delay 16 ns; Delay Ref left; Triggered.
TRIGGER	: Trig level −500 mV; Slope +ve; Atten X1; HF Sense off; HF Reject off.
DISPLAY	: Display Mode Averaged; Number of Averages 8; Screen Single; Graticule: Grid; Bandwidth 20 GHz.

Note

The above parameters may be obtained by using the Digitizing Oscilloscope *Autoscale* function and modifying as required.

9. Adjust the Digitizing Oscilloscope amplitude, timebase and delay to position the *one* bit highlighted in step 4 at the center of the display. The display below shows a typical waveform for the HP 70841B:



Ch. 1	= 200.0 mVolts/div	Offset	= -548.6 mVolts
Timebase	= 100 ps/div	Delay	= 18.9280 ns
Ch. 1 Parameters		P-P Volts	= 975.00 mVolts
Rise Time	= 93.6 ps	Fall Time	= 100.2 ps
Freq.	= 1.48854 GHz	Period	= 671.8 ps
+ Width	= 345.8 ps	- Width	= 326.0 ps
Overshoot	= 1.960 %	Preshoot	= 0.000 %
RMS Volts	= 667.92 mVolts	Dutycycle	= 51.47 %

Trigger on External at Pos. Edge at -473.5 mVolts

10. Use the Digitizing Oscilloscope *MEASUREMENT* function to check the following waveform parameters:

Measured Parameter	HP 70841B
Rise Time (10% to 90%)	< 120 ps
Rise Time (20% to 80%)	< 90 ps
Fall Time (10% to 90%)	< 120 ps
Fall Time (20% to 80%)	< 90 ps
Preshoot	< 15%
Overshoot	< 15%

Note

If poor rise and fall times are obtained, the Digitizing Oscilloscope may *NOT* be estimating the waveform 0-100% level correctly. Use the following manual procedure to check the rise and fall times manually on the Digitizing Oscilloscope.

i. Select *Delta V* then set MARKER 1 to pulse minimum and MARKER 2 to pulse maximum using the *SET MARKER 1* and *SET MARKER 2* keys.

ii. Set the marker preset levels to 10% and 90%.

iii. Select *Delta t*, then adjust the *Start Marker* to cross V MARKER 1 at the rising edge of the waveform.

iv. Adjust the *Stop Marker* to cross V MARKER 2 at the rising edge of the waveform.

v. Note the *Delta t* reading. This gives the waveform rise time.

vi. Select *Delta t*, then adjust the *Start Marker* to cross the V MARKER 2 at the falling edge of the waveform.

vii. Adjust the *Stop Marker* to cross the V MARKER 1 at the falling edge of the waveform.

viii. Note the *Delta t* reading. This gives the waveform fall time.

This manual procedure should also be used when measuring the 20-80% rise and fall times, (in step in ii set the preset level to 20-80%).

Checking Maximum Module Frequency Waveforms at the DATA OUT Port

11. Connect Channel 1 of the Four Channel Test Set to the *DATA OUT* port. Ensure that the *DATA OUT* port is terminated in 50 Ω.
12. Press `dat o/p` on the Pattern Generator then set `POLARITY NORMINV` to `INV` (inverted output). Check that the waveform is similar to that shown in step 9. Repeat step 10 then set `POLARITY NORMINV` to `NORM`.
13. Press `edit usr-pat` followed by `INTERNL PATT 1` then set the pattern to 1010 1010 1111 1111 0000 0000 1100 1100.
14. Adjust the Digitizing Oscilloscope delay to position the zero highlighted in step 13 at the center of the display.
15. Repeat step 10.

Checking 300 MHz Waveforms at the DATA OUT Port

16. Set the Synthesized Sweeper for a 300 MHz sinewave at 0 dBm.
17. Press `edit usr-pat` followed by `INTERNL PATT 1`. Set the pattern to 1010.
18. Adjust the Digitizing Oscilloscope amplitude, offset, timebase and delay to obtain a display similar to that shown in step 9.

19. Use the Digitizing Oscilloscope *MEASUREMENT* function to check the following data waveform parameters:

Measured Parameter	HP 70841B
Rise Time (10% to 90%)	<150 ps
Fall Time (10% to 90%)	<150 ps
Preshoot	<15%
Overshoot	<15%

20. Press `dat o/p` followed by **DATA AMPLTD**. Set the amplitude to 0.5 V using the numeric keys. Repeat steps 18 and 19 with the data amplitude at 0.5 V and 2 V.
21. Return the Pattern Generator Data amplitude to 1 V.

Checking 300 MHz Waveforms at the DATA OUT Port

22. Connect Channel 1 of the Four Channel Test Set to the *DATA OUT* port. Ensure that the $\overline{\mathit{DATA\ OUT}}$ port is terminated in 50Ω.
23. Repeat steps 18 to 21.

Checking Relative DATA and $\overline{\textbf{DATA}}$ Phases

24. Connect Channel 2 of the Four Channel Test Set to the Pattern Generator $\overline{\mathit{DATA\ OUT}}$ port.
25. Switch on Channel 2 of the Digitizing Oscilloscope, then set the Channel 2 parameters to match Channel 1 parameters (using *Autoscale* may ease setup).
26. Check that the *DATA OUT* and $\overline{\mathit{DATA\ OUT}}$ waveforms are 180 degrees out of phase (anti-phase).

Trigger Output Waveform and Data Output Intrinsic Jitter

Specifications

Jitter

Specified for $2^{23}-1$ PRBS, 2 V p-p output amplitude, 0 V high level and measured relative to clock/32 trigger pulse:

HP 70841B at 2.5 GHz: 10 ps rms

Trigger Output

Provides a trigger pulse synchronous with the pattern or clock. There are two modes of operation: pattern mode and clock/32 mode.

Pattern Mode: For all patterns except alternate word, the output is a 16-clock period trigger pulse synchronized to repetitions of the pattern. The rising edge of the trigger pulse is active.

PRBS Test Patterns (2^n-1): Pulse synchronized to a selectable trigger pattern n-bits long in the PRBS.

Word Test Patterns: The trigger pulse can be synchronized to any bit in the pattern.

Alternate Word Test Pattern: Trigger output changes as the word alternates under control of the auxiliary input.

Repetition Rate: PRBS $2^{31}-1$, $2^{23}-1$, $2^{15}-1$: one pulse every 16 repetitions. For all other patterns, rate is a function of the pattern length. The pulse occurs at the lowest common multiple of 128 and the length. For example, for a pattern length of 32767, the trigger pulse occurs every 128 patterns repetitions and for a pattern length of 32768, the trigger pulse occurs every pattern repetition.

Clock/32 Mode: The trigger pulse output is the input clock divided by 32.

Pulse Amplitude: Output terminated 50Ω to 0 V. High: 0 V nominal. Low: −0.75 V nominal.

Impedance: 50Ω nominal.

Interface: dc coupled.

Connector: N-type female.

Description

A Digitizing Oscilloscope is used to measure the *intrinsic jitter* on the waveforms at the Pattern Generator *DATA OUT* and $\overline{\textit{DATA OUT}}$ ports with respect to the reference *TRIGGER OUT* signal. The test is performed at the single specified pattern, clock frequency and Data amplitude. The *TRIGGER OUTPUT* signal is first checked for correct waveform parameters using the Digitizing Oscilloscope.

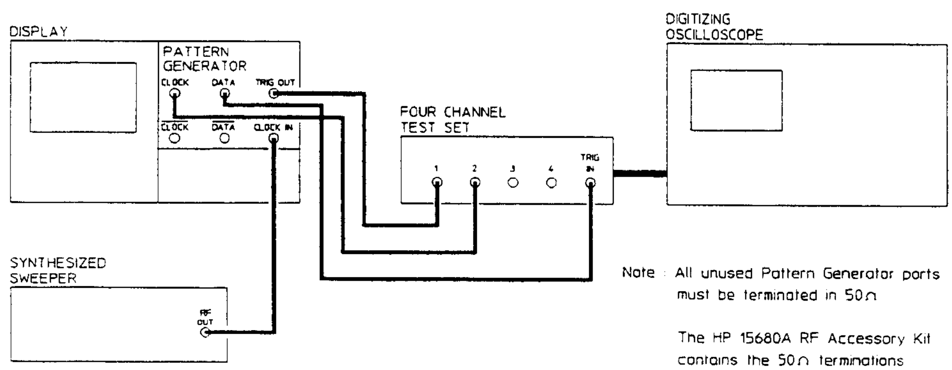
Equipment

Synthesized Sweeper	: HP 83620A
Digitizing Oscilloscope	: HP 54121T
Four Channel Test Set	: HP 54121A
RF Accessory Kit	: HP 15680A
Display	: HP 70004A

Procedure

Checking Waveform at the Trigger Out Port

1. Initialize the Pattern Generator module, see page 4-5.
2. Press `edit usr-pat` followed by `INTERNL PATT 1`. Set the pattern to 1000 0000 0000 0000 0000 0000 0000 0000 (see *Appendix B*).
3. Press `select pattern` followed by `user pattern`. Press `user pattern` again then select `INTERNL PATT 1` to transmit the pattern.
4. Press `trg o/p` then set `TRIGGER PAT CLK` to `CLK`. This enables the Pattern Generator to output a trigger pulse every 32 clock pulses.
5. Set the Synthesized Sweeper to the maximum module frequency and 0 dBm.
6. Connect the equipment as shown:

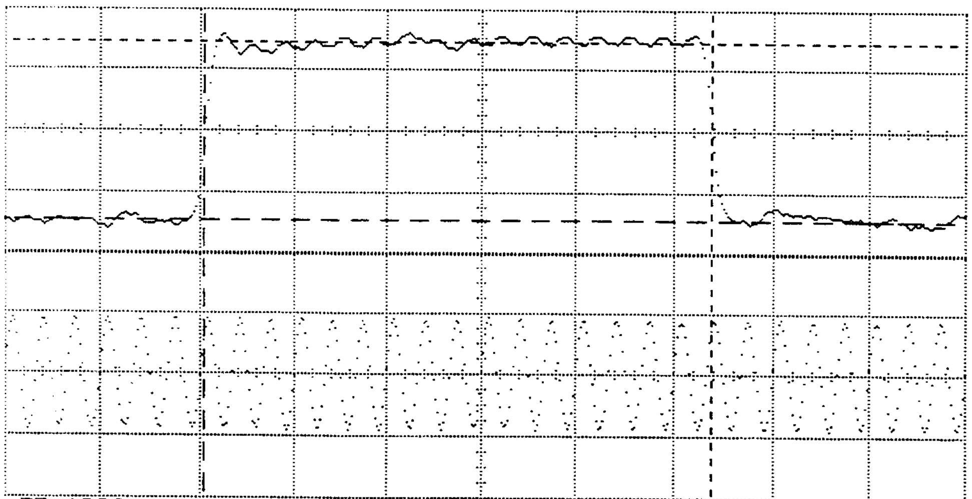


7. Set the Digitizing Oscilloscope for the following parameters:

CHAN	: Atten X1; CH 1,2 on; CH 3,4 off; CH 1 Amplitude 400 mV/Div; Offset −500 mV; CH 2 Amplitude 200 mV/div; Offset −500 mV.
TIMEBASE	: Timebase 1 ns/Div; Delay 16 ns; Delay Ref left; Triggered.
TRIGGER	: Trig level −200 mV; Slope +ve; Atten X1; HF Sense off; HF Reject off.
DISPLAY	: Display Mode Averaged; Number of Averages 8; Screen Dual; Bandwidth 20 GHz.

Note The above parameters may be obtained by using the Digitizing Oscilloscope *Autoscale* function and modifying as required.

8. Adjust the Digitizing Oscilloscope delay and timebase to display one *trigger pulse*. The display below shows a typical waveform for the HP 70841B:




```
Ch. 1       =  300.0 mVolts/div          Offset      = -472.1 mVolts
Ch. 2       =  20.00 mVolts/div          Offset      =  125.0 uVolts
Timebase    =  1.00 ns/div               Delay       =  77.1000 ns
Ch. 1 Parameters                         P-P Volts   =  956.25 mVolts
Rise Time   =  163.4   ps                Fall Time   =  175.8   ps
+ Width     =  5.3360  ns                Overshoot   =  5.405   %
Preshoot    =  4.864   %

Trigger on External at Pos. Edge at -283.0 mVolts
```

9. Check that the trigger spans 16 clock pulses. Using the Digitizing Oscilloscope delay check that the full trigger period is 32 clock pulses.

10. Adjust the Digitizing Oscilloscope timebase and delay to center one *trigger pulse* across the display.

11. Measure the amplitude and width of the displayed pulse. Typically the amplitude of the pulse will be −0.75 V (that is, *Hi* level is 0 V, *Low* level is −0.75 V) and the width will be 5.3 ns.

Checking Intrinsic Jitter at the DATA OUT Port

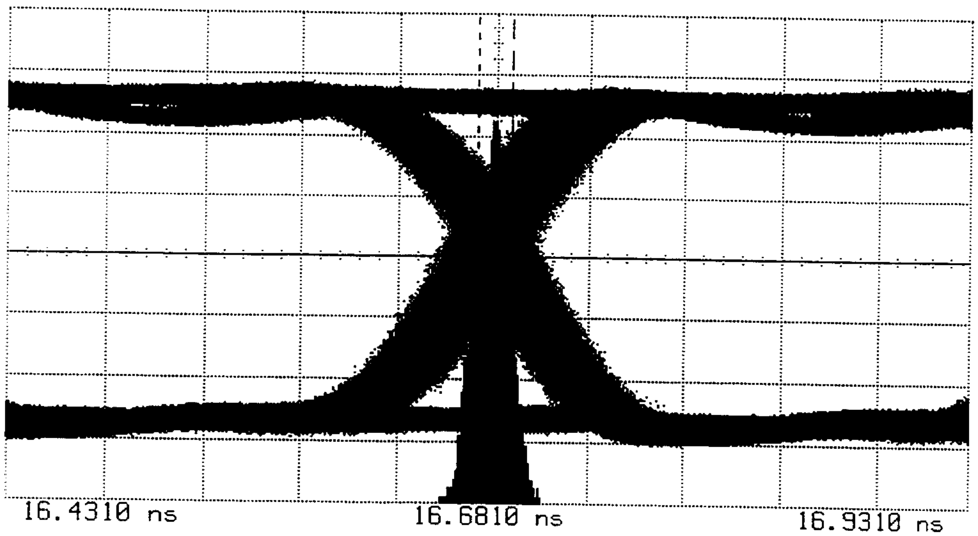
12. Connect the Pattern Generator *DATA OUT* port to Channel 1 of the Four Channel Test Set.
13. Connect the Pattern Generator *TRIGGER OUT* to the trigger Channel of the Four Channel Test Set.
14. Initialize the Pattern Generator module, see page 4-5.
15. Press `dat o/p` followed by `DATA AMPLTD`. Set the data output amplitude to 2 V using the numeric keys.
16. Press `DATA HI-LEVEL`. Set the data Hi level to 0 V using the numeric keys.
17. Press `trg o/p` and set `TRIGGER PAT CLK` to `CLK`.
18. Set the Synthesized Sweeper frequency to 2.5 GHz.
19. Set the Digitizing Oscilloscope as follows:
    i. Select the following parameters:

CHAN	: Atten X1; CH 1 on; CH 2, 3, 4 off; CH 1 Amplitude 400 mV/Div; Offset −1 V.
TIMEBASE	: Timebase 50 ps/Div; Delay 16 ns; Delay Ref left; Triggered.
TRIGGER	: Trig level −500 mV; Slope +ve; Atten X1; HF Sense off; HF Reject off.
DISPLAY	: Display Mode Persist; Persist time 300 ms; Screen single; Bandwidth 20 GHz.

Note

The above parameters may be obtained by using the Digitizing Oscilloscope *Autoscale* function and modifying as required.

ii. Adjust the timebase and delay to obtain a wavefrom similar to the following. The display below shows a typical waveform for the HP 70841B:



Ch. 1	= 200.0 mVolts/div	Offset	= -512.6 mVolts
Timebase	= 50.0 ps/div	Delay	= 16.4310 ns
Delta Windo=	0.0000 Volts		
Window 1	= -512.50 mVolts	Window 2	= -512.50 mVolts
Delta %	= 67.07 %		
Upper	= 85.36 %	Lower	= 18.29 %
Delta T	= 18.1 ps		
Start	= 16.6890 ns	Stop	= 16.6709 ns
# Samples	= 1000		
Mean	= 16.6800 ns	Sigma	= 9.0 ps

Trigger on External at Pos. Edge at -466.0 mVolts

iii. Select *HISTOGRAM* followed by *Window*.

iv. Adjust *WINDOW MARKER 1* and *WINDOW MARKER 2* to the center of the eye crossover.

v. Select *Acquire* then enter 1000 (the number of samples).

vi. Press *Start Acquiring*. The measurement ends when *100%* appears at the top left of the display.

vii. Select *Results* followed by *Sigma* to obtain the measured intrinsic jitter. This must be $<$ 10 ps RMS.

Checking Intrinsic Jitter at the $\overline{\text{DATA OUT}}$ Port

20. Repeat step 18 with Channel 1 of the Four Channel Test Set connected to the $\overline{\textit{DATA OUT}}$ port. Ensure the *DATA OUTPUT* port is terminated in 50Ω.

PRBS 2^n-1 Pattern Length

Specifications

PRBS Test Patterns:
$2^{31}-1$, polynomial $D^{31}+D^{28}+1=0$, inverted.
$2^{23}-1$, polynomial $D^{23}+D^{18}+1=0$, inverted (as in CCITT Rec O.151).
$2^{15}-1$, polynomial $D^{15}+D^{14}+1=0$, inverted (as in CCITT Rec O.151).
$2^{10}-1$, polynomial $D^{10}+D^{7}+1=0$, inverted.
$2^{7}-:1$, polynomial $D^{7}+D^{6}+1=0$, inverted.

Description

A Frequency Counter is used to verify the PRBS pattern length and the number of blocks of *ones* in each of the four preset PRBS patterns.

The clock to trigger 0/1 transition ratio measured on the Frequency Counter verifies the pattern length of each PRBS. The data to trigger 0/1 transition ratio verifies the number of *ones* in each PRBS. Because the results are ratios, they are independent of clock frequency and Frequency Counter timebase accuracy.

These two tests confirm the major specified parameters in each PRBS pattern.

Equipment

Synthesized Sweeper	: HP 83620A
Frequency Counter	: HP 5328B Option 031 (1300 MHz)
Microwave Counter	: HP 5343A
RF Accessory Kit	: HP 15680A
Display	: HP 70004A

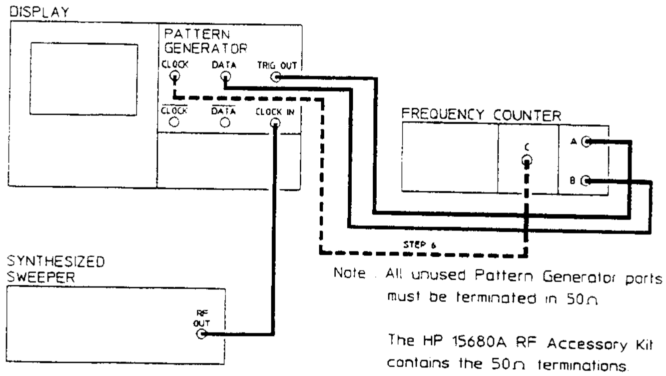
Procedure

Verifying the Number of blocks of ones in a PRBS

1. Initialize the Pattern Generator module, see page 4-5.
2. Set the Synthesized Sweeper to the minimum module frequency and 0 dBm.
3. Set the Frequency Counter as follows:

Ratio	: B/A
CH A	: Slope +, Atten 1, Termination 50 Ω
CH B	: Slope +, Atten 1, Termination 50 Ω
Scale (N)	: 10

4. Connect the equipment as shown:



5. Press `select pattern` then set the Pattern Generator to the PRBS patterns listed in the following table. Check that the Frequency Counter readings match those listed in the table. The Frequency Counter scale factor (N) must be set to obtain the required resolution. It may be necessary to adjust the Frequency Counter sensitivity to obtain stable readings.

PRBS Pattern	Counter Reading
2^7-1	4096.0 ±0.1
$2^{10}-1$	32768.0 ±0.1
$2^{15}-1$	131072.0 ±0.1
$2^{23}-1$	33554432.0 ±0.1

Note

A trigger output pulse occurs every 128 patterns on PRBS 2^7-1 and PRBS $2^{10}-1$, and every 16 patterns on $2^{15}-1$, $2^{23}-1$ and $2^{31}-1$.

Verifying PRBS Pattern Length

6. Connect a cable from the Pattern Generator *CLOCK OUTPUT* to Channel C of the Frequency Counter (*90 MHz-1.3 GHz* port).
7. Set the Frequency Counter to *Ratio C/A*.
8. Set the Pattern Generator to the PRBS patterns listed in the following table, check that the Frequency Counter readings match those listed in the table. The Frequency Counter scale factor (N) must be set to obtain the required resolution. It may be necessary to adjust the Frequency Counter sensitivity to obtain stable readings. The Frequency Counter will take several seconds to make a measurement on the longer patterns.

PRBS Pattern	Counter Reading
2^7-1	16256.0 ±0.1
$2^{10}-1$	130944.0 ±0.1
$2^{15}-1$	524272.0 ±0.1
$2^{23}-1$	(1)34217712.0 ±0.1

Note

A trigger output pulse occurs every 128 patterns on PRBS 2^7-1 and every 16 patterns on PRBS $2^{10}-1$, $2^{15}-1$, $2^{23}-1$ and $2^{31}-1$.

9. Repeat step 8 with the Synthesized Sweeper set to 1 GHz at 0 dBm.
10. Replace the Frequency Counter with the Microwave Counter.
11. Connected the Pattern Generator *TRIGGER OUTPUT* port to the 10 Hz-500 MHz input on the Microwave Counter (call this Channel A). Channel A must also have its 1 MΩ termination selected.
12. Connect the Pattern Generator *CLOCK OUTPUT* to the 500 MHz-26.5 GHz input on the Microwave Counter (call this Channel B).
13. Press `select pattern` followed by `2^7-1`.
14. Set the Synthesized Sweeper to 3 GHz.
15. Measure and note the frequency on Channel A.
16. Measure and note the frequency on Channel B.
17. Calculate the ratio B/A. Ensure it is 16256.0 ±0.1.
18. Repeat steps 13 - 17 for $2^{10}-1$, $2^{15}-1$ and $2^{23}-1$

PRBS 2^n Variable Mark Density

Specifications

Variable Mark Density Test Patterns:

2^{13}, polynomial $D^{13}+D^{12}+1=0$
2^{11}, polynomial $D^{11}+D^{9}+1=0$
2^{10}, polynomial $D^{10}+D^{7}+1=0$
2^{7}, polynomial $D^{7}+D^{6}+1=0$

In the above patterns an extra zero is added to extend the longest run of zeros by one.

The ratio of ones to total bits in the above patterns can be set to 1/8, 1/4, 1/2, 3/4 and 7/8.

Description

A Frequency Counter is used to verify the pattern length and the number of *ones* in each of the four preset PRBS patterns with a variable Mark Density of 1/8, 1/4, 1/2, 3/4, 7/8.

The clock to trigger 0/1 transition ratio measured on the Frequency Counter verifies the pattern length of each PRBS. The data to trigger 0/1 transition ratio verifies the number of *ones* in each PRBS. Because the results are ratios, they are independent of clock frequency and Frequency Counter timebase accuracy.

Equipment

Synthesized Sweeper	: HP 83620A
Frequency Counter	: HP 5328B Option 031 (1300 MHz)
Microwave Counter	: HP 5343A
RF Accessory Kit	: HP 15680A
Display	: HP 70004A

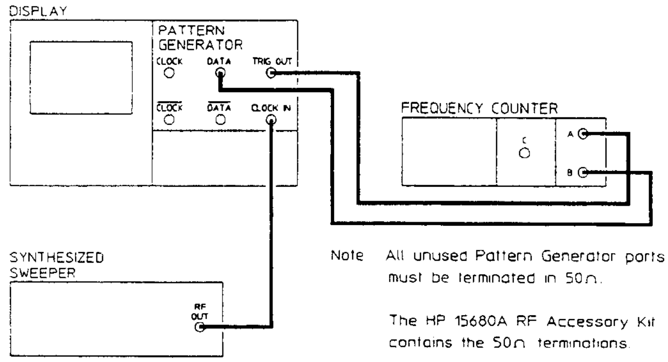
Procedure

Verifying the Number of Ones in the PRBS

1. Initialize the Pattern Generator module, see page 4-5.
2. Set the Synthesized Sweeper to the minimum module frequency and 0 dBm.
3. Set the Frequency Counter as follows:

Ratio	: B/A
CH A	: Slope +, Atten 1, Termination 50Ω
CH B	: Slope +, Atten 1, Termination 50Ω
Scale (N)	: 10

4. Connect the equipment as shown on the following page:



5. Press `select pattern` then use `more 1 of 3` to display `more 3 of 3`. Set the Pattern Generator PRBS pattern and mark density ratio as listed in the following table, and check that the Frequency Counter readings match those listed. The Frequency Counter scale factor (N) must be set to obtain the required resolution. It may be necessary to adjust the Frequency Counter sensitivity to obtain stable readings.

PRBS Pattern	Mark Density Ratio	Counter Reading
2^7 MARKDEN	1/8	16.0 ±0.1
2^7 MARKDEN	1/4	32.0 ±0.1
2^7 MARKDEN	1/2	32.0 ±0.1
2^7 MARKDEN	3/4	16.0 ±0.1
2^7 MARKDEN	7/8	8.0 ±0.1
2^{10} MARKDEN	1/8	112.0 ±0.1
2^{10} MARKDEN	1/4	192.0 ±0.1
2^{10} MARKDEN	1/2	256.0 ±0.1
2^{10} MARKDEN	3/4	192.0 ±0.1
2^{10} MARKDEN	7/8	112.0 ±0.1
2^{11} MARKDEN	1/8	224.0 ±0.1
2^{11} MARKDEN	1/4	384.0 ±0.1
2^{11} MARKDEN	1/2	512.0 ±0.1
2^{11} MARKDEN	3/4	384.0 ±0.1
2^{11} MARKDEN	7/8	224.0 ±0.1
2^{13} MARKDEN	1/8	896.0 ±0.1
2^{13} MARKDEN	1/4	1536.0 ±0.1
2^{13} MARKDEN	1/2	2048.0 ±0.1
2^{13} MARKDEN	3/4	1536.0 ±0.1
2^{13} MARKDEN	7/8	896.0 ±0.1

Note

There is a trigger output pulse at the end of every pattern on all the above PRBS rates.

Verifying the Pattern Length

6. Connect the Pattern Generator *CLOCK OUTPUT* port to Channel C of the Frequency Counter (90 MHz-1.3 GHz port).
7. Set the Frequency Counter to *Ratio C/A*.
8. Set the Pattern Generator to the PRBS patterns listed in the following table, and check that the Frequency Counter readings match those listed. The Frequency Counter scale factor (N) must be set to obtain the required resolution. It may be necessary to adjust the Frequency Counter sensitivity to obtain stable readings.

PRBS Pattern	Counter Reading
2^7 MARKDEN	128.0 ±0.1
2^{10} MARKDEN	1024.0 ±0.1
2^{11} MARKDEN	2048.0 ±0.1
2^{13} MARKDEN	8192.0 ±0.1

Note There is a trigger output pulse at the end of every pattern on all the above PRBS rates.

9. Repeat step 8 with the Synthesized Sweeper set to 1 GHz at 0 dBm.
10. Replace the Frequency Counter with the Microwave Counter.
11. Connect the Pattern Generator *TRIGGER OUTPUT* to the 10 Hz-500 MHz input on the Microwave Counter (call this Channel A). Channel A must also have its 1 MΩ termination selected.
12. Connect the Pattern Generator *CLOCK OUTPUT* to the 500 MHz-26.5 GHz input on the Microwave Counter (call this Channel B).
13. Set the Synthesized Sweeper to 3 GHz.
14. Set the Pattern Generator PRBS pattern to 2^7 **MARKDEN**.
15. Measure and note the frequency on Channel A.
16. Measure and note the frequency on Channel B.
17. Calculate the ratio B/A. Ensure it is 128.0 ±0.1.

18. Set the Pattern Generator to the PRBS patterns listed in the following table, repeat steps 15 to 17 at each PRBS. The expected ratio B/A at each PRBS is listed in the following table.

PRBS Pattern	B/A Ratio
2^{10} MARKDEN	1024.00 ±0.1
2^{11} MARKDEN	2048.00 ±0.1
2^{13} MARKDEN	8192.00 ±0.1

PRBS 2^n Zero Substitution

Specifications

Zero Substitution Test Patterns:

2^{13}, polynomial $D^{13}+D^{12}+1=0$
2^{11}, polynomial $D^{11}+D^{9}+1=0$
2^{10}, polynomial $D^{10}+D^{7}+1=0$
2^{7}, polynomial $D^{7}+D^{6}+1=0$

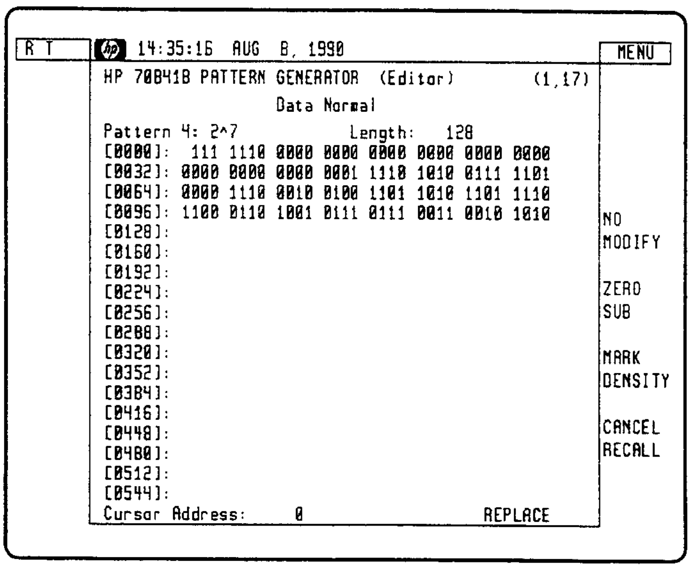
In the above patterns an extra zero is added to extend the longest run of zeros by one.

Zeros can be substituted for data to extend the longest run of zeros in the above patterns. The longest run can be extended to the pattern length, minus one. The bit after the substituted zeros is set to 1.

Description

A Frequency Counter is used to verify the number of ones in each of the four preset PRBS patterns across the full zero substitution range.

The Data to Trigger 0/1 transition ratio verifies the number of *ones* in each PRBS. This will decrease as the longest run of *zeros* in the pattern is increased. An example of *zero substitution* is shown below for 2^7PRBS. In the following example the longest run of zeros is set to 40.



Equipment

Synthesized Sweeper : HP 83620A
Frequency Counter : HP 5328B Option 031 (1300 MHz)
RF Accessory Kit : HP 15680A
Display : HP 70004A

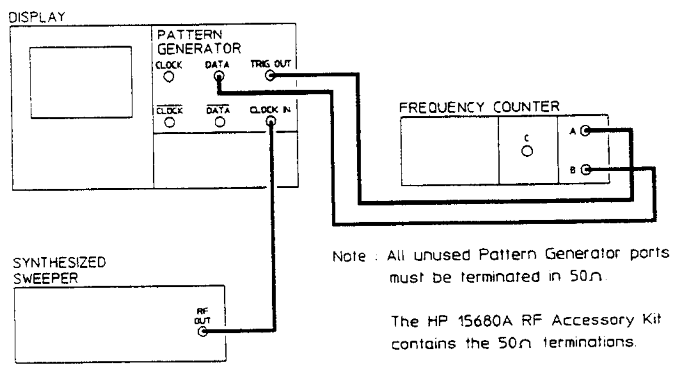
Procedure

Verifying the Number of Ones in a PRBS

1. Initialize the Pattern Generator, see page 4-5.
2. Set the Synthesized Sweeper to the minimum module frequency and 0 dBm.
3. Set the Frequency Counter as follows:

Ratio	: B/A
CH A	: Slope +, Atten 1, Termination 50Ω
CH B	: Slope +, Atten 1, Termination 50Ω
Scale (N)	: 10

4. Connect the equipment as shown:



5. Press `select pattern` followed by `more 1 of 3` to display `more 2 of 3` and `LONGEST RUNZERO`. Set the PRBS pattern and the longest run of zeros to those listed in the following table. Check that the Frequency Counter readings match those shown. The Frequency Counter scale factor (N) must be set to obtain the required resolution. It may be necessary to adjust the Frequency Counter sensitivity to obtain stable readings.

PRBS Pattern	Longest Run of Zeros	Counter Reading
2^7 ZEROSUB	7 to 11	32.0 ±0.1
2^7 ZEROSUB	24 to 29	28.0 ±0.1
2^7 ZEROSUB	40 to 43	24.0 ±0.1
2^7 ZEROSUB	55 to 59	20.0 ±0.1
2^7 ZEROSUB	72 to 74	16.0 ±0.1
2^7 ZEROSUB	83 to 87	12.0 ±0.1
2^7 ZEROSUB	99 to 100	8.0 ±0.1
2^7 ZEROSUB	114 to 115	4.0 ±0.1
2^7 ZEROSUB	120 to 127	1.0 ±0.1
2^{10} ZEROSUB	10 to 15	256.0 ±0.1
2^{10} ZEROSUB	161 to 162	220.0 ±0.1
2^{10} ZEROSUB	320 to 322	180.0 ±0.1
2^{10} ZEROSUB	471 to 473	140.0 ±0.1
2^{10} ZEROSUB	637 to 640	100.0 ±0.1
2^{10} ZEROSUB	783 to 789	60.0 ±0.1
2^{10} ZEROSUB	925 to 927	20.0 ±0.1
2^{10} ZEROSUB	1022 to 1023	1.0 ±0.1
2^{11} ZEROSUB	11 to 18	512.0 ±0.1
2^{11} ZEROSUB	237 to 239	450.0 ±0.1
2^{11} ZEROSUB	636 to 643	350.0 ±0.1
2^{11} ZEROSUB	1065 to 1073	250.0 ±0.1
2^{11} ZEROSUB	1463 to 1466	150.0 ±0.1
2^{11} ZEROSUB	1854 to 1855	50.0 ±0.1
2^{11} ZEROSUB	2038 to 2039	5.0 ±0.1
2^{11} ZEROSUB	2046 to 2047	1.0 ±0.1
2^{13} ZEROSUB	13 to 20	2048.0 ±0.1
2^{13} ZEROSUB	1833 to 1836	1600.0 ±0.1
2^{13} ZEROSUB	3365 to 3368	1200.0 ±0.1
2^{13} ZEROSUB	4946 to 4949	800.0 ±0.1
2^{13} ZEROSUB	6616 to 6617	400.0 ±0.1
2^{13} ZEROSUB	7795 to 7796	100.0 ±0.1
2^{13} ZEROSUB	8148 to 8152	10.0 ±0.1
2^{13} ZEROSUB	8188 to 8191	1.0 ±0.1

Error Add

Specifications

Error Add

There are three modes of operation: Single errors on demand; External Errors (injected via the rear panel input) and Selectable Fixed error ratios of 1 error in 10^3, 10^4, 10^5, 10^6, 10^7, 10^8 and 10^9 bits.

Description

A Frequency Counter is used to verify that errors are added into the transmitted data when the *single error add* and *fixed error rate* functions are used.

With the Pattern Generator transmitting an *all zeros* word, the Frequency Counter reading will increment by one each time the Pattern Generator **ERR-ADD SINGLE** key is pressed. With the Pattern Generator *Fixed Error Rates* selected, there is one errored data bit every 10^X bits (with X being selectable between 3 and 9). The Frequency Counter is used to verify this by measuring the data to trigger ratio on all zeros pattern .

Equipment

Synthesized Sweeper	:	HP 83620A
Frequency Counter	:	HP 5328B Option 031 (1300 MHz)
RF Accessory Kit	:	HP 15680A
Display	:	HP 70004A

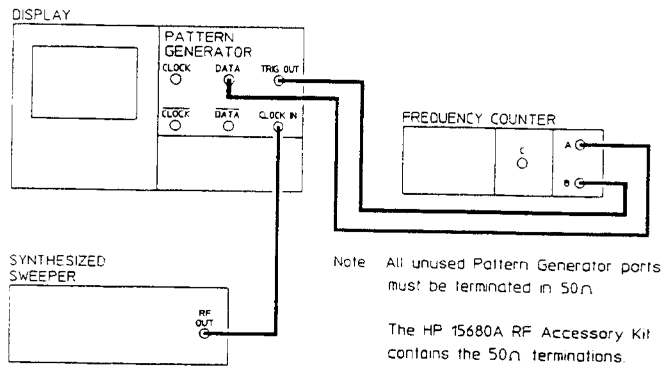
Procedure

Single Error Add

1. Initialize the Pattern Generator module, see page 4-5.
2. Set the Synthesized Sweeper to the minimum module frequency and 0 dBm.
3. Set the Frequency Counter as follows:

START	:	A
Scale (N)	:	1

4. Connect the equipment as shown:



5. Press edit usr-pat followed by INTERNL PATT 1 . Set the pattern to 0000 0000 0000 0000 (see *Appendix B*).
6. Press select pattern followed by user pattern . Press user pattern again then select INTERNL PATT 1 .
7. Press trg o/p then set TRIGGER PAT CLK to CLK .
8. Set the Frequency Counter to *START* mode with a scaling factor (N)=1.
9. Press the Frequency Counter (RESET) key.
10. Press err-add then more 1 of 2 to display more 2 of 2 followed by error add (right side of display). Press ERR-ADD SINGLE once. Check that the Frequency Counter reading increments to 1. It may be necessary to adjust the Frequency Counter sensitivity.
11. Check that the Frequency Counter reading increments by one each time the ERR-ADD SINGLE key is pressed.
12. Repeat steps 9 to 11 with the Synthesized Sweeper set to 1 GHz.

Fixed Error Rate

13. Set the Synthesized Sweeper to the minimum module frequency and 0 dBm.
14. Press ERR-ADD FIXED then fixed rate on the right of the display followed by 1e-6 .
15. Set the Counter to *Ratio B/A* with scaling factor (N)=10^3.
16. Check that the counter reading is 31250.00 ±0.1. It may be necessary to adjust the Frequency Counter sensitivity to obtain stable readings.

17. Set the `fixed rate` on the Pattern Generator to each of the values shown below, check that the Counter reading matches in each case:

Error-add Rate	Counter Reading
1e−3	31.25 ±0.1
1e−4	312.5 ±0.1
1e−5	3125 ±0.1
1e−7	312,500 ±0.1
1e−8	3,125,000 ±0.1
1e−9	31,250,000 ±0.1

18. Repeat step 17 with the Synthesized Sweeper set to 1 GHz.

User Selectable Patterns Disc Memory Backup

Specifications

Variable Length User Test Patterns (RAM stored)

Length: 1 to 4,194,304 bits

Resolution:
1 bit to 32,768 bits in 1 bit steps
32,768 to 65,536 bits in 2 bit steps
65,536 to 131,072 bits in 4 bit steps
131,072 to 262,144 bits in 8 bit steps
262,144 to 524,288 bits in 16 bit steps
524,288 to 1,048,576 bits in 32 bit steps
1,048,576 to 2,097,152 bits in 64 bit steps
2,097,152 to 4,194,304 bits in 128 bit steps

Four internal RAM stores are provided for user patterns. Each store can hold one pattern up to 4,194,304 bits.

Description

A Digitizing Oscilloscope is used to ensure that the Pattern Generator can produce four predefined *User Selectable Patterns* at the maximum module frequency. A Frequency Counter in the ratio mode verifies that the patterns selected have the correct ratio of *ones* to *Pattern Trigger* in accordance with the rules given in the specifications above. The patterns used provide maximum stress to the Pattern Generator circuitry. The ratios are checked with clock frequencies of 100 MHz and 1 GHz.

Memory backup is checked by powering down the system and verifying that the four *User Selectable Patterns* stored in RAM are unchanged when the system is powered up.

Equipment

Synthesized Sweeper	: HP 83620A
Digitizing Oscilloscope	: HP 54121T
RF Accessory Kit	: HP 15680A
Display	: HP 70004A

Procedure

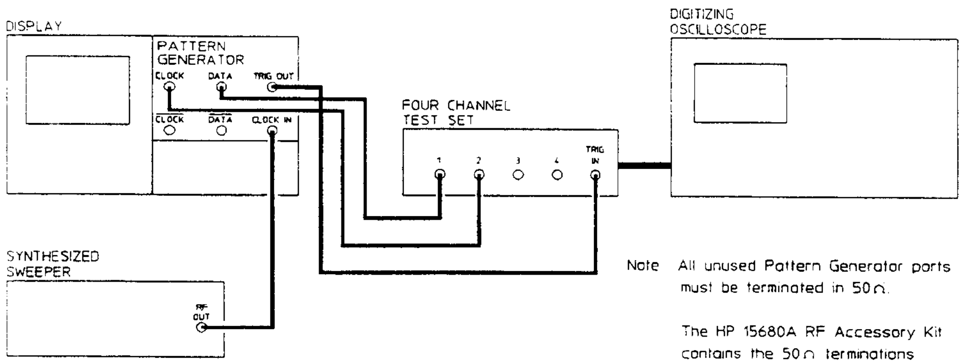
Checking User Patterns on the Digitizing Oscilloscope

1. Initialize the Pattern Generator module, see page 4-5.

2. Press `edit usr-pat` then edit each pattern as follows (see *Appendix B*):

INTERNL PATT 1	1001 0111 0010 110 (pattern length of 15 bits)
INTERNL PATT 2	1111 1111 1111 1110 1111 1111 1111 1111 0000 0000 0000 0001 0000 0000 0000 0000 (pattern length of 64 bits)
INTERNL PATT 3	1010 (repeat for pattern length of 255 bits)
INTERNL PATT 4	1 (pattern length of 1 bit)

3. Set the Synthesized Sweeper to the maximum module frequency and 0 dBm.
4. Connect the equipment as shown:

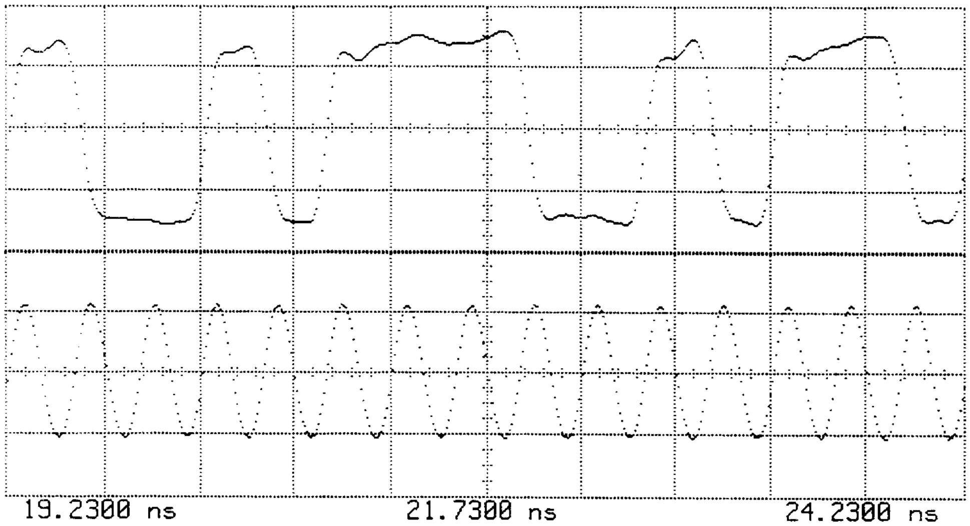


5. Set the Digitizing Oscilloscope for the following parameters:

CHAN	: Atten X3; CH 1 on; CH 2 on; CH 3,4 off; CH 1,2 Amplitude 160 mV/Div; CH 1 Offset −236 mV; CH 2 Offset 0 mV.
TIMEBASE	: Timebase 1 ns/Div; Delay 1 ns; Delay Ref left; Triggered.
TRIGGER	: Trig level −500 mV; Slope +ve; Atten X1; HF Sense off; HF Reject off.
DISPLAY	: Display Mode Averaged; Number of Averages 8; Screen Dual; Graticule grid; Bandwidth 20 GHz.

6. Press `select pattern` followed by `user pattern`. Press `user pattern` again then select `INTERNL PATT 1`.

7. Adjust the Digitizing Oscilloscope timebase and delay (as required) to obtain a display similar to the following. Ensure the data displayed on Channel 1 agrees with that set up as `INTERNL PATT 1` (NRZ format) by counting the number of *ones* and *zeros*.

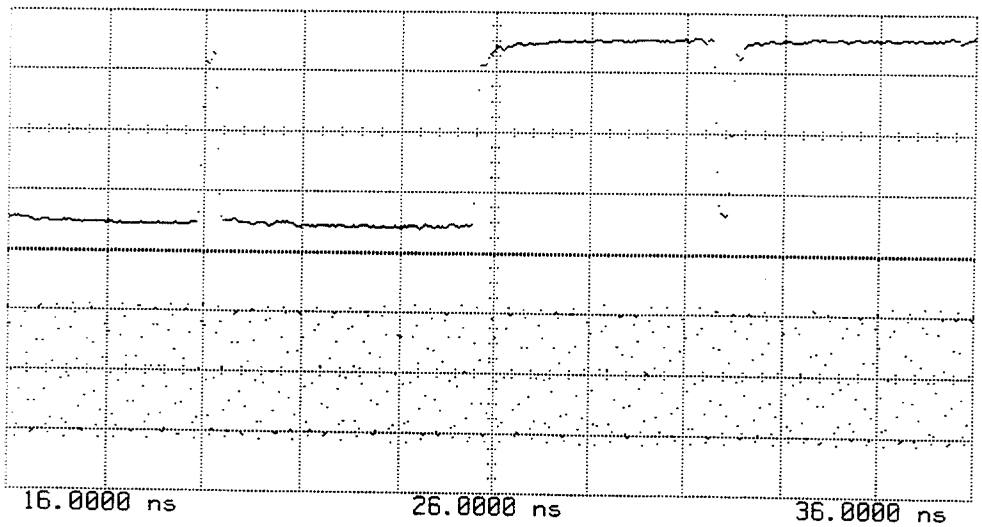


Ch. 1	=	160.0 mVolts/div	Offset	=	-236.2 mVolts
Ch. 2	=	160.0 mVolts/div	Offset	=	1.250 mVolts
Timebase	=	500 ps/div	Delay	=	19.2300 ns

Trigger on External at Pos. Edge at -481.0 mVolts

8. Press `User Patter` followed by `INTERNL PATT 2`.

9. Adjust the Digitizing Oscilloscope timebase and delay (as required) to obtain a display similar to the following. Ensure the data displayed on Channel 1 agrees with that set up as INTERNL PATT 2 (NRZ format) by counting the number of *ones* and *zeros*.

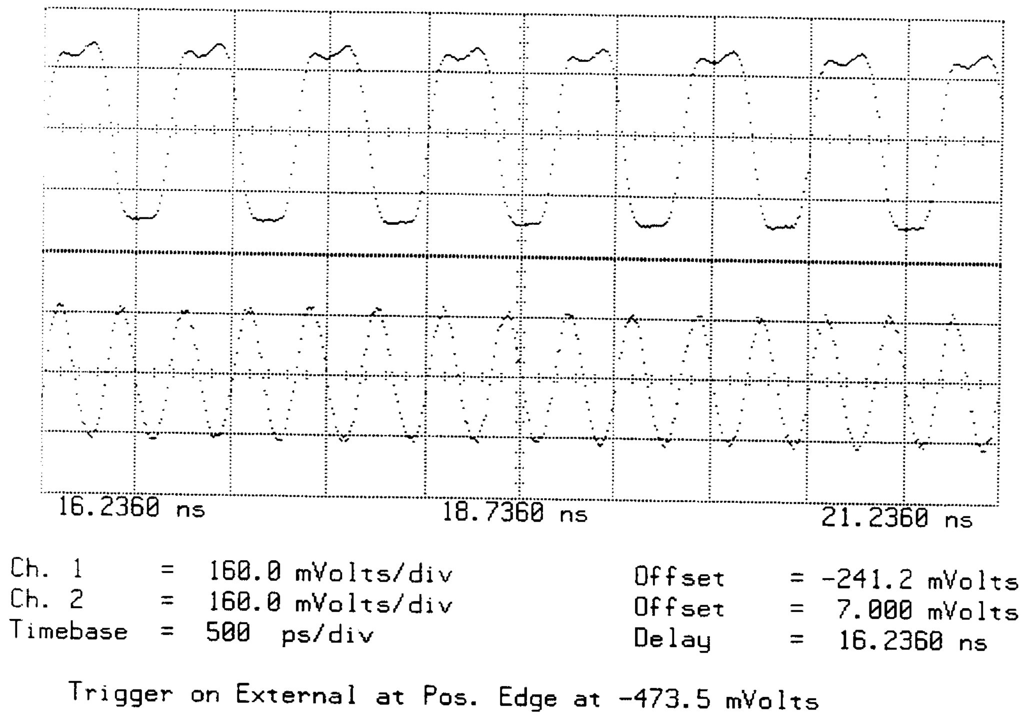


Ch. 1	=	160.0 mVolts/div	Offset	=	-241.2 mVolts
Ch. 2	=	160.0 mVolts/div	Offset	=	7.000 mVolts
Timebase	=	2.00 ns/div	Delay	=	16.0000 ns

Trigger on External at Pos. Edge at -473.5 mVolts

10. Press User Pattern followed by INTERNL PATT 3.

11. Adjust the Digitizing Oscilloscope timebase and delay (as required) to obtain a display similar to the following. Ensure the data displayed on Channel 1 agrees with that set up as INTERNL PATT 3 (NRZ format) by counting the number of *ones* and *zeros*.

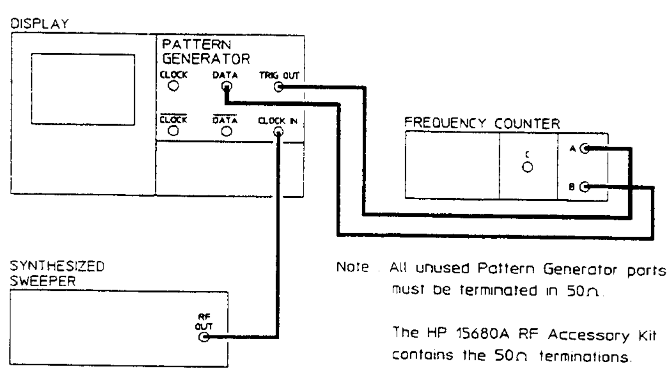


12. Press **User Pattern** followed by **INTERNL PATT 4**.

13. The Digitizing Oscilloscope display should be a DC level of typically +1 V.

Checking User Patterns on the Frequency Counter

14. Connect the equipment as shown:



15. Set the Synthesized Sweeper to the minimum module frequency and 0 dBm.

16. Set the Frequency Counter as follows:.

Ratio	: B/A
CH A	: Slope +, Atten 1, Termination 50Ω
CH B	: Slope +, Atten 1, Termination 50Ω
Scale (N)	: 10

17. Select INTERNL PATT 1 to INTERNL PATT 4 in turn and ensure that the counter readings match those shown. It may be necessary to adjust the counter sensitivity to obtain stable readings.

User Pattern	Counter Reading
INTERNL PATT 1	640 ±0.1
INTERNL PATT 2	6 ±0.1
INTERNL PATT 3	16256 ±0.1
INTERNL PATT 4	No Reading (DC)

18. Set the Synthesized Sweeper to 1 GHz at 0 dBm.
19. Connect a cable from the Pattern Generator *DATA OUTPUT* port to Channel C of the Frequency Counter (*90 MHz-1.3 GHz* port).
20. Set the Frequency Counter to Ratio C/A.
21. Set the Pattern Generator to INTERNL PATT 1 to INTERNL PATT 4 in turn and ensure that the counter readings match those shown in step 17.

Memory Backup

22. Switch off the Display using the *LINE* switch.
23. Wait a few seconds, then switch on the Display.
24. Set the Pattern Generator to INTERNL PATT 1 to INTERNL PATT 4 in turn and ensure that the counter readings match those shown in step 17.

Disc Drive Test

Specifications

Description

The pattern generator disc drive is checked to ensure that it can format a blank floppy disc. Then a check is made to ensure that patterns of various length can be saved from the current pattern to floppy disc and retreived from floppy disc back into the current pattern.

Equipment

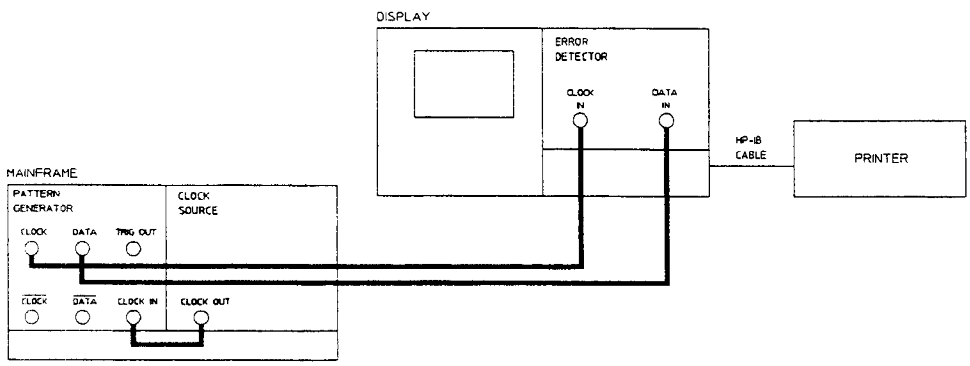
The following equipment will be required for these tests.

1. HP 70004 display
2. HP 70842B error detector
3. HP XXXX accessory kit
4. HP 2225A printer
5. HP xxxx HP-IB cable

Procedure

Disc formatting test

1. Connect the equipment as shown below and initialise the pattern generator as explained on page 4-5.



2. Press the **misc** softkey and install a blank high density 3.5 inch floppy disc in the disc drive.
3. Press the **format disc** softkey at he bottom of the right hand menu followed by the **Format** key on the menu that follows. This key will now be highlighted with a flashing "yes" beneath it. A "Formatting disc - please wait" message will be visible at the bottom of the display and the led on the disc drive will be on.

Formatting a disc takes a few minutes after which time the disc drive led will be off and the display will show the main pattern generator menu as in step 1.

Pattern save test

1. Press the `edit usr-pat` softkey followed by the `more` softkey.
2. Press the `load block` softkey followed by the 2^7 `prbs` softkey.
3. Press the `set pat length` softkey and key in the value 127.
4. Press the `set pat label` softkey. Use the PRG control and left hand menu softkeys to give the new pattern a specific label.
5. Press the `PRINT` key on the front panel of the display. A printout of this pattern and its attributes will appear. This printout will be used in the **Retrieve pattern test** section for comparison with the retrieved patterns.
6. Press the `save pattern` softkey followed by the `disc patt 5` softkey.
7. Press the `select pattern` softkey followed by the `user pattern` softkey. Note that the display shows the label and the length of the new pattern which you have just saved.

Note

Steps 1 to 7 are to be repeated for user patterns `disc patt 6` to `disc patt 12` using different prbs sequences to load the current pattern. Different pattern lengths and labels should also be assigned to each pattern.

Pattern retrieve test

1. Press the `select pattern` softkey followed by the `user patterns` softkey.
2. Press the `DISC PATT 5` softkey. Disc pattern 5 will now be loaded into the current pattern file in the pattern generator.
3. Press the `select pattern` softkey followed by the `current pattern` softkey.
4. Press the `edit usr-pat` softkey followed by the `current pattern` softkey. Note that the label (upper lefthand side of the display), pattern length (bottom of the display) and pattern content are identical to that in the printout of the previous section.

Note

Repeat steps 1 to 4 above for disc patterns 6 to 12.

Auxiliary Input Test

Specifications

Auxiliary Input

Provides a means of controlling the alternate pattern changeover or forcing the data output to zero.

Alternate Pattern Selected: The input signal forces a change between the two patterns at the end of either pattern. One of two modes can be chosen:

Oneshot: A rising edge on the input (minimum pulse width) inserts a single version of B into repetitions of A.

Alternate: The logic state of the input determines which pattern is output. (A logic *0* will output pattern A.)

Alternate Pattern Not Selected: The input signal forces the data output to TTL high.

Levels: TTL compatible, active low.

Pulse Width:

Clock	Minimum Pulse Width
$\geq$ 500 MHz	100 ns
100 to 500 MHz	250 ns

Interface: dc coupled.

Description

With *PRBS Pattern* selected on the Pattern Generator, a Digitizing Oscilloscope is used to verify that a TTL low level (active) at the rear panel *AUXILIARY INPUT* port inhibits the PRBS pattern at the *DATA OUT* port (all bits to zero).

With Alternate Word selected, a Frequency Counter is used to verify that a TTL Low level at the rear panel *AUXILIARY INPUT* port selects PATTERN A and a TTL high selects PATTERN B. The TTL signal at the *AUXILIARY INPUT* port is a pulse set to the minimum width specified for the Clock Frequency in use and is supplied by the Pulse Generator. With *PATTERN A* set to *all ones* and *PATTERN B* set to *all zeros* the changeover frequency of the Data Out signal will be the same as the Auxiliary Input pulse rate. The Frequency Counter measures these two signals in the *RATIO* mode ensure results are independent of Pulse Generator frequency and Frequency Counter timebase.

Equipment

Synthesized Sweeper	: HP 83620A
Digitizing Oscilloscope	: HP 54121T
RF Accessory Kit	: HP 15680A
Display	: HP 70004A
Frequency Counter	: HP 5343A
Pulse Generator	: HP 8116A
Power Splitter	: HP 11667A

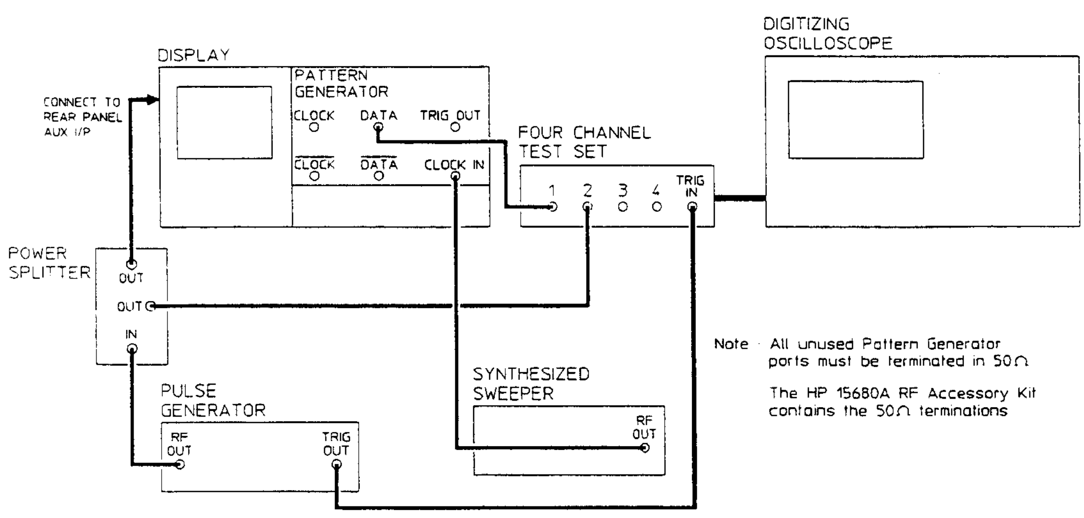
Procedure

Checking Pattern Inhibit

1. Initialize the Pattern Generator module, see page 4-5.
2. Set the Synthesized Sweeper to the minimum module frequency and 0 dBm.
3. Set the Pulse Generator as follows:

Waveform	: Pulse
Pulse Width	: 250 ns
Frequency	: 2 MHz
Amplitude	: 5 V peak-to-peak
Offset	: 0 V

4. Connect the equipment as shown in the following diagram:



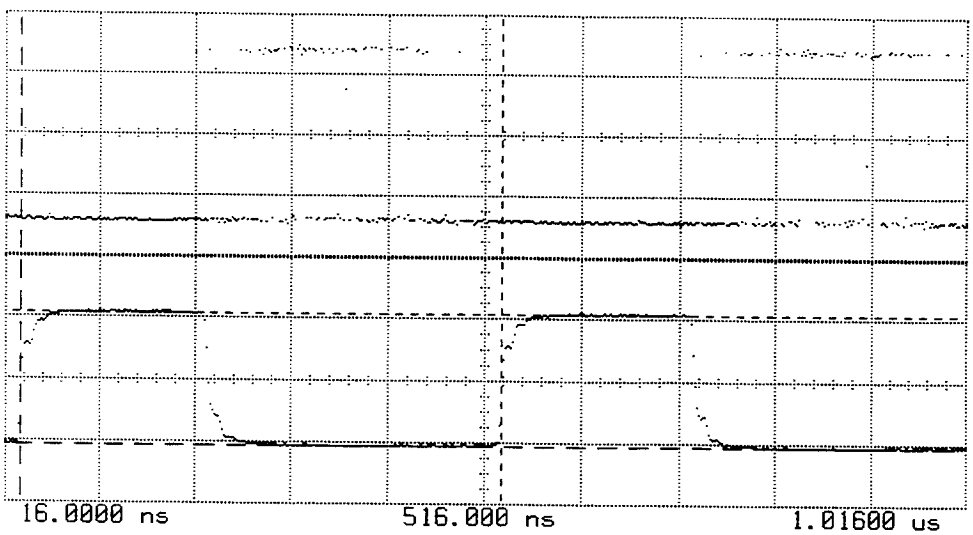
5. Set the Digitizing Oscilloscope for the following parameters:

CHAN	: Atten X1; CH 1 on; CH 2 on ;CH 3,4 off; CH 1 Amplitude 300 mV/Div; CH 1 Offset −500 mV; CH 2 Amplitude 1.6 V/div; CH 2 Offset 0 V.
TIMEBASE	: Timebase 100 ns/Div; Delay 16 ns; Delay Ref left; Triggered.
TRIGGER	: Trig level 500 mV; Slope +ve; Atten X1; HF Sense off; HF Reject off.
DISPLAY	: Display Mode Averaged; Number of Averages 8; Screen Dual; Graticule grid; Bandwidth 20 GHz.

Note

The above parameters may be obtained by using the Digitizing Oscilloscope *Autoscale* function and modifying as required.

6. Adjust the Digitizing Oscilloscope timebase, delay and range to obtain a waveform similar to the following. The display shows a typical waveform for the HP 70841B.




```
Ch. 1       =  300.0 mVolts/div          Offset    = -422.2 mVolts
Ch. 2       =  1.600  Volts/div          Offset    =  0.000  Volts
Timebase    =  100  ns/div               Delay     =  16.0000 ns
Delta V     =  3.4000  Volts
Vmarker1    = -1.6750  Volts             Vmarker2  =  1.7250  Volts
Delta T     =  501.919 ns
Start       =  32.5908 ns                Stop      =  534.509 ns

     Trigger on External at Pos. Edge at  99.00 mVolts
```

7. Ensure that the PRBS pattern is present at the *DATA OUT* port *for the same length of time* that the pulse signal is high and is inhibited *for the same length of time* that the pulse signal is low (active).

Note

Due to delays within the Pattern Generator the *AUX IN* and *Data Output* signals will not be coincident.

8. Repeat steps 6 to 7 with the Pulse Generator frequency and pulse width and the Synthesized Sweeper frequency set to the values shown:

Pulse Generator		**Synthesized Sweeper**
Frequency	*Pulse Width*	*Frequency*
2 MHz	250 ns	499 MHz
5 MHz	100 ns	500 MHz
5 MHz	100 ns	1 GHz
5 MHz	100 ns	3 GHz

Checking Alternate Word Select

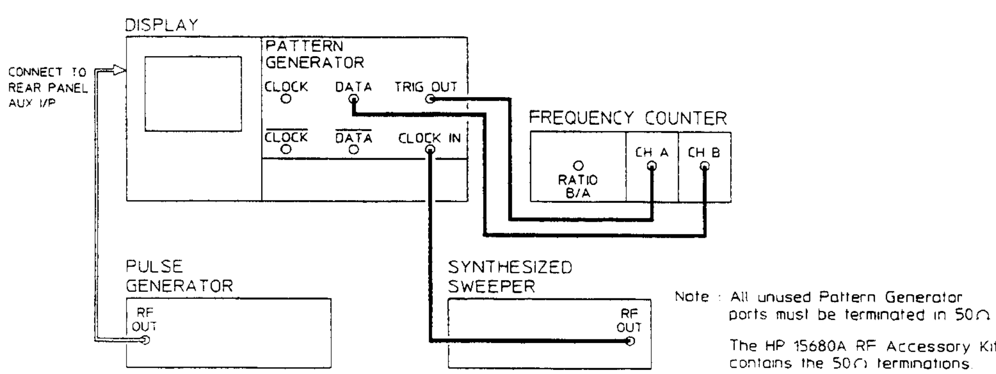
9. Set the Synthesized Sweeper to the minimum module frequency and 0 dBm.
10. Set the Pulse Generator as follows:

Waveform	: Pulse
Pulse Width	: 250 ns
Frequency	: 2 MHz
Amplitude	: 5 V peak-to-peak
Offset	: 0 V

11. Set the Frequency Counter as follows:

Ratio	: B/A
CH A	: Slope +, Atten 1, Termination 50Ω
CH B	: Slope +, Atten 1, Termination 50Ω
Scale (N)	: 10

12. Connect the equipment as follows:



13. Press `select pattern` followed by `more 1 of 3` to display `more 2 of 3`. Press `alt word` twice then set WORD 0 to 11111111 11111111 and WORD 1 to 00000000 00000000.

14. Adjust the Frequency Counter CH A and B sensitivity controls for a stable reading of 1.0 ±0.1.

15. Repeat steps 14 with the Pulse Generator frequency and pulse width and the Synthesized Sweeper frequency set to the values shown:

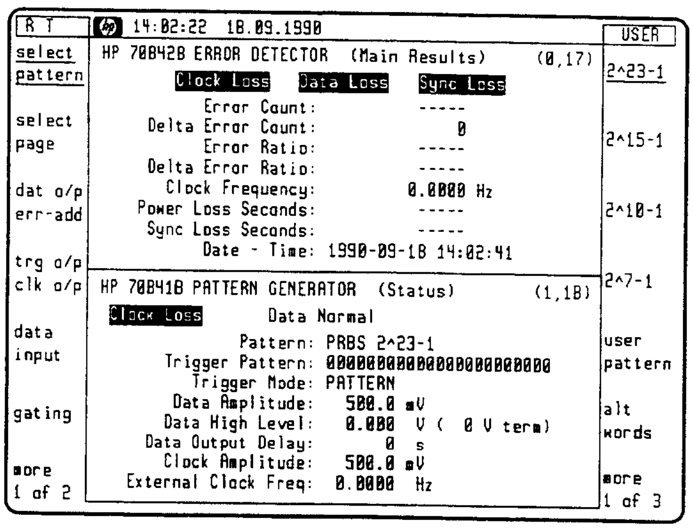
Pulse Generator		Synthesized Sweeper
Frequency	*Pulse Width*	*Frequency*
2 MHz	250 ns	499 MHz
5 MHz	100 ns	500 MHz
5 MHz	100 ns	1 GHz
5 MHz	100 ns	3 GHz

Error Detector Performance Tests

These tests (on pages 4-52 to 4-91) ensure that the HP 70842B 0.1 - 3 GHz Error Detector modules meet specification. The Error Detector performance checks require the system to be configured either *master/master* or *master/slave* prior to performance testing, see the *Preliminary Procedures* on the following pages.

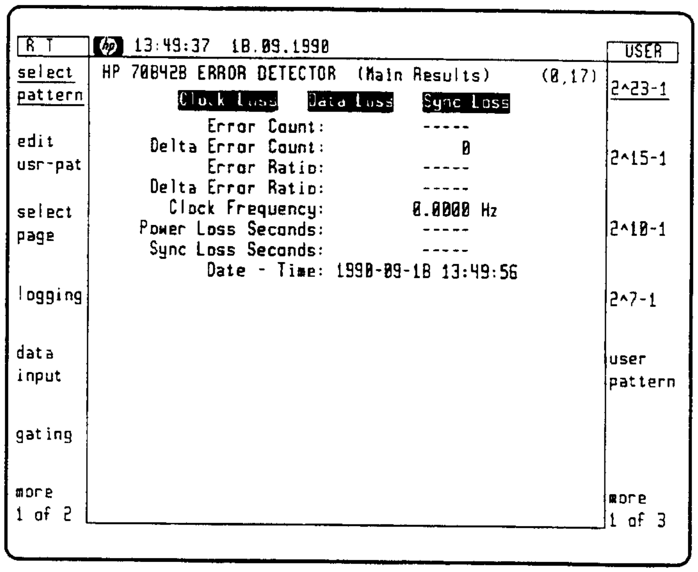
Error Detector Module Preliminary Setup (Master/Slave)

1. Interconnect the *HP-MSIB IN* and *OUT* ports on the HP 70004A Display and the HP 70001A Mainframe, see page 2-13.
2. Note the Error Detector module *HP-MSIB address* (row and column), it must be returned to this setting after its performance has been verified.
3. Set the Error Detector module *row address* to 0 and *column address* to 17, see page 2-7.
4. Set the Pattern Generator module *row address* to 1 and the *column address* to 18, see page 2-8.
5. Plug the Error Detector module (to be tested) into the Display and the Pattern Generator module into the Mainframe.
6. Power-on the Display and Mainframe (system selftest occurs at power-on, takes approximately 15 seconds complete).
7. Press (DISPLAY) followed by **NEXT INST** to establish a communication link between the Error Detector module and the Display.
8. Press (INST PRESET) to initialize the Error Detector and Pattern Generator modules (to their preset or default settings). A typical display is shown below:



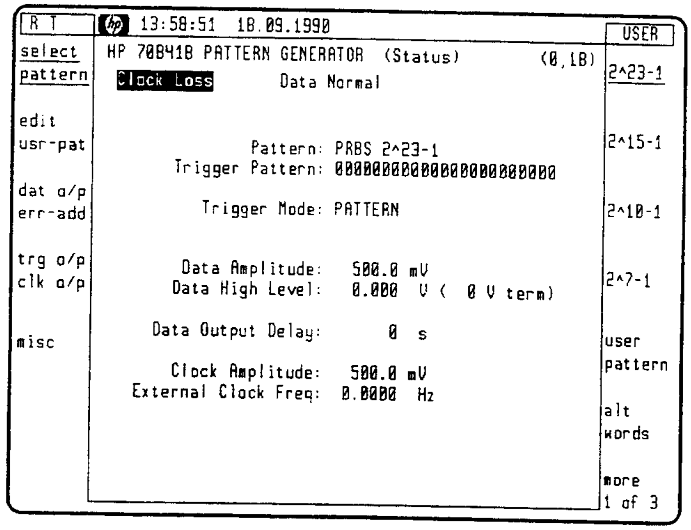
Preliminary Setup (Master/Master)

1. Interconnect the *HP-MSIB IN* and *OUT* ports on the HP 70004A Display and the HP 70001A Mainframe, see page 2-13.
2. Note the Error Detector module *HP-MSIB address* (row and column), it must be returned to this setting after its performance has been verified.
3. Set the Error Detector module *row address* to 0 and *column address* to 17, see page 2-7.
4. Set the Pattern Generator module *row address* to 0 and the *column address* to 18, see page 2-8.
5. Plug the Error Detector module (to be tested) into the Display and the Pattern Generator module into the Mainframe.
6. Power-on the Display and Mainframe (system selftest occurs at power-on, takes approximately 15 seconds to complete).
7. Press (DISPLAY) followed by **NEXT INST** until the Error Detector parameters appear on the display.
8. Initialize the Error Detector module to its preset or default settings, by pressing (INST PRESET). A typical Error Detector display is shown below:



9. Press (DISPLAY) followed by **NEXT INST** to establish a communication link between the Pattern Generator module and the Display - the Pattern Generator parameters should appear on the display.

10. Initialize the Pattern Generator module to its preset or default settings, by pressing INST PRESET. A typical display is shown below:



Clock Input Levels

Specifications

Waveform: Compatible with the following:
Clock Sources: HP 70322A or HP 70311A.
Signal Generators: HP 8665A or HP 8644A.
Pattern Generator Modules: HP 70841A/B

Amplitude: ±4 dBm.

Return Loss: Typically > 10 dB over the operating range.

Impedance: 50Ω nominal.

Interface: dc coupled.

Connector: N-type female.

Alternative clock Sources: Other clock sources offering a similar performance to those listed under *Waveform* can be used provided they meet the following:
Noise: SSB broadband noise floor, offsets > 10 MHz from the carrier in the range 10 MHz to 4 GHz:

Carrier Frequency	Noise floor
< 300 MHz	< −140 dBc/Hz
> 300 MHz	< −130 dBc/Hz

Maximum Power from 50Ω Source: 15 dBm.

Description

This test ensures that the Error Detector can synchronize to a worst-case test pattern with the *CLOCK IN* signal set to minimum and maximum specified amplitudes. The Clock Loss alarm functions on the Error Detector are also checked in this test.

The *CLOCK IN* signal for the Pattern Generator is provided by a Synthesized Sweeper via a Power Splitter and for the Error Detector via another Power Splitter with the Power Meter used to measure the signal level at the Error Detector *CLOCK IN* port. This level is first adjusted to the minimum clock input level specified - the Error Detector is then monitored to ensure correct alignment across the full frequency range with a specific *User Selectable Pattern* set up on both the Pattern Generator and Error Detector. The clock polarity is inverted as required to achieve this. The above test is repeated with the Synthesized Sweeper amplitude set to the maximum level specified for the Error detector *CLOCK IN* port. The Clock Loss alarms are verified by reducing the Synthesized Sweeper level until these alarms are displayed on the Error Detector. The level at which this occurs is noted.

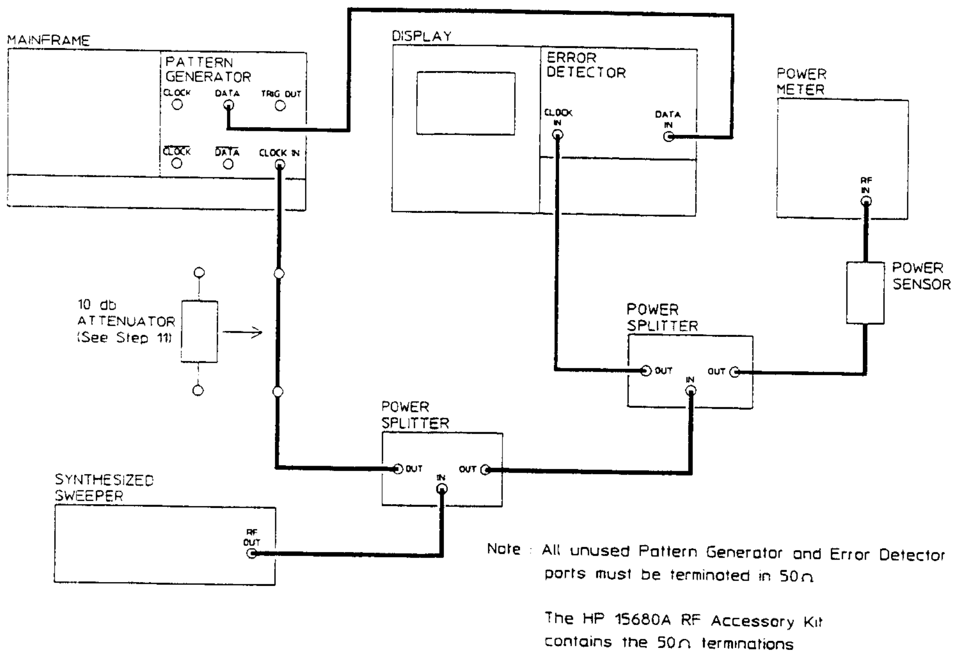
Equipment

Synthesized Sweeper : HP 83620A
RF Accessory Kit : HP 15680A
Pattern Generator : HP 70841A/B
Display : HP 70004A
Power Meter : HP 436A
Power Sensor : HP 8482A
Power Splitter : HP 11667A (2 required)
Attenuator : HP 8491A (option 010)

Procedure

Pattern Alignment

1. Initialize the Error Detector and Pattern Generator as a master/slave system, see page 4-52.
2. Connect the equipment as shown:



Note Use only cables from the RF Accessory Kit to connect the Pattern Generator to the Error Detector. These cables are of equal length and type and have optimum characteristics for the following tests.

3. Set the Power Meter to read *dBm* (100% CAL factor).

Note The Power Sensor should be calibrated using the Power Meter internal Power Reference. Refer to the Power Meter Operating Manual for details.

4. Set the Synthesized Sweeper to the minimum module frequency and adjust the level for −4 dBm as read on the Power Meter.
5. Press `more 1 of 2` followed by `edit usr-pat` then set `INTERNL PATT 1` to 1111 1111 1111 1111 0000 0000 0000 0000 (pattern length 32 bits)
6. Press `more 2 of 2` on the left of the display then press `select pattern`. Press `user pattern` twice then select `INTERNL PATT 1`.
7. Ensure that the Error Detector *CLK LOSS*, *DATA LOSS*, *SYNC LOSS* or *ERRORS* alarm indicators are not lit. Also check that the `Clock Loss`, `Data Loss`, `Sync Loss` or `Errors` alarm messages are not on the display.
8. Sweep the Synthesized Sweeper slowly between the minimum and maximum module frequency (maintain −4 dBm reading on the Power Meter) and monitor for Clock Loss, Data Loss, Sync Loss or Errors alarms. If a Sync Loss or Errors alarm occurs at any frequency, select `data input` then press `CLKEDGE NEG`. Check for pattern re-alignment, no alarm message on the display and no module alarm indicators.
9. Return the Synthesized Sweeper frequency to the minimum module frequency.

Checking Clock Loss Alarms

10. Reduce the Synthesized Sweeper level until the *CLK LOSS* alarm indicator on the Error Detector module is lit. The `Clk Loss` alarm message should appear on the display. Typically, Clock Loss alarms occur below −10 dBm. Confirm this level on the Power Meter.

Checking the Maximum Level at the Error Detector CLOCK IN Port

11. Insert the 10 dB Fixed Attenuator between the Power Splitter output and the Pattern Generator CLOCK IN port.
12. Increase the Synthesized Sweeper amplitude to obtain a reading of +4 dBm on the Power Meter.
13. Sweep the Synthesized Sweeper slowly between the minimum and maximum module frequency (maintain the +4dBm reading on the Power Meter) and monitor for Clock Loss, Data Loss, Sync Loss or Errors alarms. If a Sync Loss or Errors alarm occur at any frequency, select `data input` then press `CLKEDGE NEG`. Check for pattern re-alignment, no alarm message on the display and no module alarm indicators.

PRBS 2^n-1 Pattern Synchronization, Error Detect and Audible Indicator

Specifications

PRBS Test Patterns

$2^{31}-1$, polynomial $D^{31}+D^{28}+1=0$, inverted.
$2^{23}-1$, polynomial $D^{23}+D^{18}+1=0$, inverted (as in CCITT Rec O.151).
$2^{15}-1$, polynomial $D^{15}+D^{14}+1=0$, inverted (as in CCITT RecO.151).
$2^{10}-1$, polynomial $D^{10}+D^{7}+1=0$, inverted.
$2^{7}-1$, polynomial $D^{7}+D^{6}+1=0$, inverted.

Error Measurements

The error detector counts bit errors by comparing the incoming data bit-by-bit with the internally-generated reference pattern. All measurements run during the gating periods as described with the exception of Delta Error Count and Delta Error Ratio. These measurements run continuously to facilitate user adjustments for minimizing errors.

Error Count: The total number of errors during the gating period.

Delta Error Count: The number of errors in successive decisecond intervals.

Error Ratio: The ratio of counted errors to the number of bits in the selected gating period.

Delta Error Ratio: The ratio of counted errors to the number of bits in successive decisecond intervals.

Errored Intervals: Time intervals during which one or more errors occurred. These intervals are errored seconds, deciseconds, centiseconds or milliseconds.

Error Free Intervals: Time intervals of seconds, deciseconds, centiseconds or milliseconds, during which no errors occurred.

Description

This test ensures that the Error Detector can synchronize to 2^7-1, $2^{10}-1$, $2^{15}-1$, $2^{23}-1$ and $2^{31}-1$ PRBS patterns and can also count *single* and *fixed rate* bit errors on each pattern.

A Pattern Generator is set to transmit each pattern - the Error Detector is monitored to ensure correct alignment on each pattern across the full frequency range. The active clock edge on the Error Detector is inverted as required to achieve this.

Single errors are then added to each transmitted pattern - the Error Detector is checked to ensure these errors are detected. Finally, the Pattern Generator is set to a fixed error rate - the Error Detector is checked for the correct error rate and result analysis on each pattern. Single and fixed error rates are verified at three discrete frequencies.

The audible indicator is verified by listening for a beep each time errors are added.

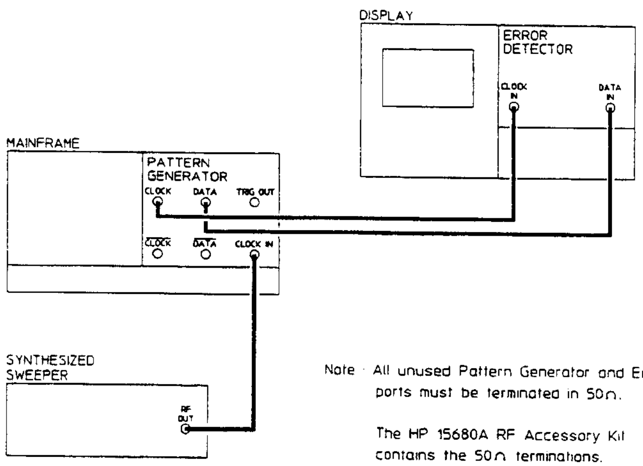
Equipment

Synthesized Sweeper	: HP 83620A
RF Accessory Kit	: HP 15680A
Pattern Generator	: HP 70841A/B
Display	: HP 70004A

Procedure

Pattern Alignment

1. Initialize the Pattern Generator and Error Detector as a master/slave system, see page 4-52.
2. Set the Synthesized Sweeper to the minimum module frequency and 0 dBm.
3. Connect the equipment as shown:



Note

Use only cables from the HP 15680A RF Accessory Kit to connect the Pattern Generator to the Error Detector. These cables are of equal length and type and have optimum characteristics for the following tests.

4. Ensure that the Error Detector *CLK LOSS*, *DATA LOSS*, *SYNC LOSS* or *ERRORS* alarm indicators are not lit. Also check that the `Clock Loss`, `Data Loss`, `Sync Loss` or `Errors` alarm messages are not on the display.
5. Sweep the Synthesized Sweeper slowly between the mimimum and maximum module frequencies and ensure no alarm indicators or messages occur.

   If a sync loss or errors alarm occurs at any frequency, select `data input`, then press **CLKEDGE NEG**. Check for pattern re-alignment, no alarm message on the display and no module alarm indicators.
6. Repeat step 5 with `select pattern` set to $2^{31}-1$, $2^{15}-1$, $2^{10}-1$ and $2^{7}-1$ respectively.

7. Return the Synthesized Sweeper frequency to the minimum module frequency then select `CLKEDGE POS` on the display.

Single Error Add and Audible Error Indicator

8. Press `more 1 of 2` then `misc` on the left of the display.
9. Select `BEEP ON ERROR` to activate the audible error indicator.
10. Press `more 2 of 2` followed by `gating`, then on the left of the display, select `MANUAL UNTIMED`.
11. Press `RUN GATING` (ensure the *GATING* indicator on the Error Detector module lights).
12. Select `err-add`, `more 1 of 2`, `error add` then press `ERR-ADD SINGLE` once. An audible beep should be heard.
13. Ensure that the displayed `Error Count` is 1.
14. Check that the `Error Count` increments by 1 count each time `ERR-ADD SINGLE` is pressed. The `Errors` alarm message and indicator should flash momentarily and the Beeper should sound each time an error is added.
15. Select `gating` then press `STOP GATING`, `RUN GATING` and `STOP GATING` in sequence to reset the error count to zero.
16. Repeat steps 11 to 15 with `select pattern` set to $2^{10}-1$, $2^{15}-1$, $2^{23}-1$ and $2^{31}-1$ respectively.
17. Return `select pattern` to 2^7-1 then repeat steps 11 to 16 with the Synthesized Sweeper set to the maximum module frequency.

Note If a Sync Loss alarm occurs at this frequency, press `data input` then select `CLKEDGE NEG`. Ensure that the alarm disappears.

---

18. Return the Synthesized Sweeper to the minimum module frequency then select `CLKEDGE POS` on the display. Ensure all alarms disappear.

Fixed Error Add Rate

19. Press `select page` then `MAIN RESULTS` to display `Error Count`, `Delta Error Count`, `Error Ratio` and `Delta Error Ratio`.
20. Select `err-add` followed by `more 1 of 2` on the right of the display `error add` then `ERR-ADD FIXED` and set the fixed rate to `1e-6` (one error in 10^6 bits).
21. Ensure that the `Errors` alarm message is displayed and that the *ERRORS* alarm indicator is lit. A continuous beeping should be audible.
22. Press `gating` then select `SINGLE`. Set the `GATING PERIOD` to 5 seconds using the numeric keys.

23. Press `gating` then select `RUN GATING` (ensure that the Error Detector *GATING* indicator lights).
24. Wait for gating to finish then note the `Error Ratio` and `Delta Error Ratio` readings on the display. These will be typically 1.000e-06.
25. Repeat steps 23 and 24 with `select pattern` set to $2^{23}-1$, $2^{15}-1$, $2^{10}-1$ and 2^7-1 respectively. The results will be unchanged.
26. Return the pattern to $2^{31}-1$.
27. Repeat steps 23 to 26 with the Frequency Synthesizer set to 3 GHz.

Note

If a Sync Loss alarm occurs at this frequency, press `data input` then select `CLKEDGE NEG` . Ensure that the alarm disappears.

PRBS 2^n Pattern Synchronization, Error Detect and Memory Backup

Specifications

Variable Mark Density Test Patterns:

2^{13}, polynomial $D^{13}+D^{12}+1=0$
2^{11}, polynomial $D^{11}+D^{9}+1=0$
2^{10}, polynomial $D^{10}+D^{7}+1=0$
2^{7}, polynomial $D^{7}+D^{6}+1=0$

In the above patterns an extra zero is added to extend the longest run of zeros by one.

Error Measurements

The error detector counts bit errors by comparing the incoming data bit-by-bit with the internally-generated reference pattern. All measurements run during the gating periods as described with the exception of Delta Error Count and Delta Error Ratio. These measurements run continuously to facilitate user adjustments for minimizing errors.

Error Count: The total number of errors during the gating period.

Delta Error Count: The number of errors in successive decisecond intervals.

Error Ratio: The ratio of counted errors to the number of bits in the selected gating period.

Delta Error Ratio: The ratio of counted errors to the number of bits in successive decisecond intervals.

Errored Intervals: Time intervals during which one or more errors occurred. These intervals are errored seconds, deciseconds, centiseconds or milliseconds.

Error Free Intervals: Time intervals of seconds, deciseconds, centiseconds or milliseconds, during which no errors occurred.

Description

This test ensures that the Error Detector can synchronize to 2^7, 2^{10}, 2^{11} and 2^{13} PRBS patterns and can also count *single* and *fixed rate* bit errors on each pattern.

A Pattern Generator is set to transmit each pattern - the Error Detector is monitored to ensure correct alignment on each pattern across the full frequency range. The active clock edge on the Error Detector is inverted as required to achieve this.

Single errors are then added to each transmitted pattern - the Error Detector is checked to ensure these are detected. Finally, the Pattern Generator is set to a fixed error rate of 1×10^{-5} - The Error Detector is checked for the correct error rate and results analysis. Single and fixed error rates are verified at frequency extremes.

The internal memory backup is verified by cycling the power and ensuring that the displayed clock time and date are still valid. With gating active the power is cycled - the Error Detector display is checked to ensure that the `Power Loss Seconds` has been correctly recorded (the time during which the measurement is inactive).

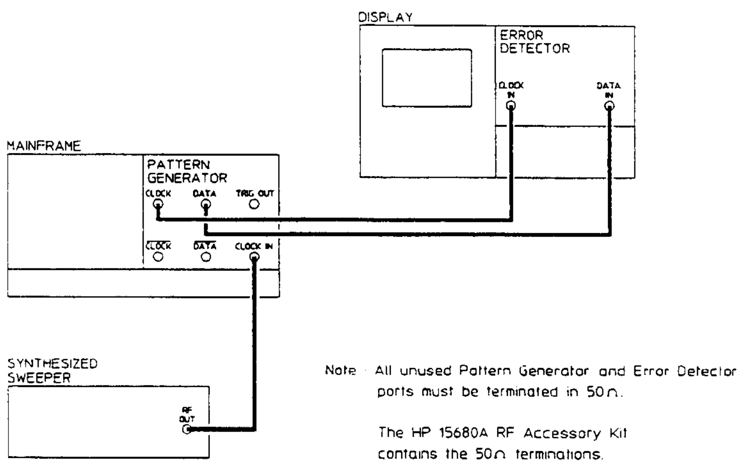
Equipment

Synthesized Sweeper : HP 83620A
RF Accessory Kit : HP 15680A
Pattern Generator : HP 70841A/B
Display : HP 70004A

Procedure

Pattern Alignment

1. Initialize the Error Detector and Pattern Generator as a master/slave system, see page 4-52.
2. Set the Synthesized Sweeper to the minimum module frequency and 0 dBm.
3. Connect the equipment as shown;



Note

Use only cables from the HP 15680A RF Accessory Kit to connect the Pattern Generator to the Error Detector. These cables are of equal length and type and have optimum characteristics for the following tests.

4. Press `select pattern` then use `more 1 of 3` until `more 3 of 3` is displayed then select 2^7 `MARKDEN`.
5. Ensure that the Error Detector *CLK LOSS*, *DATA LOSS*, *SYNC LOSS* and *ERRORS* alarm indicators are not lit. Also check that the `Clock Loss`, `Data Loss`, `Sync Loss` and `Errors` alarm messages are not on the display.
6. Sweep the Synthesized Sweeper slowly between the minimum and maximum module frequencies and monitor the module and display for Clock Loss, Data Loss, Sync Loss or Errors alarms.

   If Sync Loss or Errors indicators appear at any frequency, select `data input`, then press `CLKEDGE NEG`. Wait for resync to occur (up to 30 seconds) then check for pattern realignment, no alarm messages on the display and no module alarm indicators.

7. Repeat step 6 with `select pattern` set to 2^{10} `MARKDEN` , 2^{11} `MARKDEN` , and 2^{13} `MARKDEN` respectively.
8. Return the Synthesized Sweeper frequency to the minimum module frequency then select `CLKEDGE POS` on the display.

Single Error Add

9. Press `gating` then select `MANUAL UNTIMED` .
10. Press `RUN GATING` .
11. Select `err-add` , `more 1 of 2` , `error add` then press `ERR-ADD SINGLE` .
12. Ensure that the display `Error Count` is 1.
13. Check that the `Error Count` increments by 1 count each time `ERR-ADD SINGLE` is pressed. The `Errors` alarm message and indicator should flash momentarily each time an error is added.
14. Select `gating` then press `STOP GATING` , `RUN GATING` and `STOP GATING` in sequence to reset the error count to zero.
15. Repeat steps 10 to 14 with `select pattern` set to 2^{11} `MARKDEN` , 2^{10} `MARKDEN` and 2^{7} `MARKDEN` respectively.
16. Repeat steps 10 to 15 with the Synthesized Sweeper set to the maximum module frequency.

Note If a Sync Loss alarm occurs at this frequency, select `data input` then press `CLKEDGE NEG` . Wait for resync to occur (up to 30 seconds).

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17. Return the Synthesized Sweeper frequency to the minimum module frequency, then select `CLKEDGE POS` on the display, ensure that all alarms disappear.

Fixed Error Add Rate

18. Press `select page` then `MAIN RESULTS` to display `Error Count`, `Delta Error Count`, `Error Ratio` and `Delta Error Ratio`.
19. Select `err-add` then press `more 1 of 2` on the right of the display `error add` followed by `ERR-ADD FIXED` and set the fixed rate to `1e-5` (one error in 10^5 bits).
20. Ensure that the `Errors` alarm message is displayed and that the *ERRORS* alarm indicator is lit.
21. Press `gating` then select `SINGLE` . Set the `GATING PERIOD` to 5 seconds using the numeric keys.
22. Press `gating` then select `RUN GATING` (ensure the Error Detector *GATING* indicator is lit).

23. Wait for gating to finish then note the Error Ratio and Delta Error Ratio readings on the display. These will be typically 1.00e−5.
24. Repeat steps 22 and 23 with select pattern set to 2^{10} MARKDEN , 2^{11} MARKDEN and 2^{13} MARKDEN respectively. The results will be unchanged.

Note do not select RUN GATING until resync has occurred (up to 30 seconds).

25. Return the pattern to 2^7 MARKDEN.
26. Repeat steps 22 to 25 with the Synthesized Sweeper set to 3 GHz.

Note If a Sync Loss alarm occurs at this frequency, select data input then press CLKEDGE NEG . Wait for the resync to occur (up to 30 seconds), ensure that all alarms disappear.

Power Loss Indicator and Internal Memory Backup

27. Note the time and date shown on the display.

Note If required, refer to the *HP 71600 Series Operating Manual* for details on the setting the internal clock time and date.

28. Press gating followed by RUN GATING then switch off the Display using the *LINE* switch.
29. Switch on the Display then wait for the time and date to appear - check that the internal clock has been operating during power down.
30. Check the Power Loss Seconds on the display.

PRBS 2^n with Variable Mark Density

Specifications

Variable Mark Density Test Patterns:

2^{13}, polynomial $D^{13}+D^{12}+1=0$
2^{11}, polynomial $D^{11}+D^{9}+1=0$
2^{10}, polynomial $D^{10}+D^{7}+1=0$
2^{7}, polynomial $D^{7}+D^{6}+1=0$

In the above patterns an extra zero is added to extend the longest run of zeros by one.

The ratio of ones to total bits in the above patterns can be set to 1/8, 1/4, 1/2, 3/4 and 7/8.

Description

This test ensures that the Error Detector can synchronize to 2^7, 2^{10}, $2^{11}$and 2^{13}PRBS patterns with mark densities of 1/8, 1/4, 1/2, 3/4 and 7/8.

A Pattern Generator is set to transmit each pattern - the Error Detector is monitored to ensure correct alignment across the full frequency range. The active clock edge on the Error Detector is inverted as required to achieve this.

The Error Detector Data Threshold (the level at which the 0 to 1 transition occurs) is then adjusted manually to optimize transition point for the chosen transmit levels. The mark density can now be increased from minimum to maximum - the Error Detector alignment is verified at each mark density setting by adding single errors.

This last step is repeated at each PRBS and at frequency extremes.

Equipment

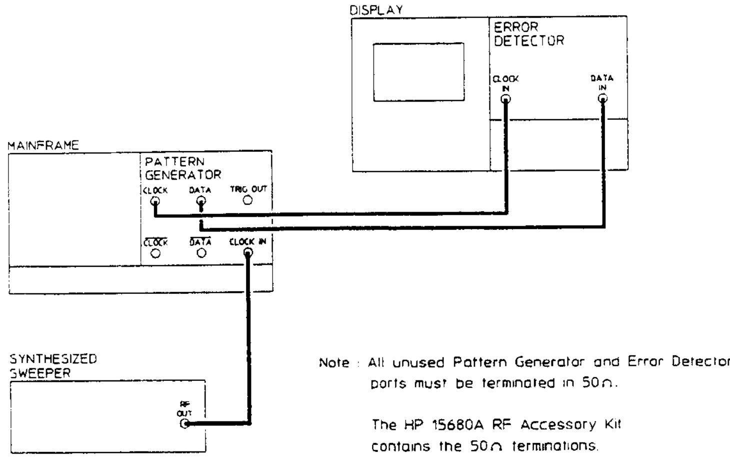
Synthesized Sweeper	: HP 83620A
RF Accessory Kit	: HP 15680A
Pattern Generator	: HP 70841A/B
Display	: HP 70004A

Procedure

Pattern Alignment

1. Initialize the Error Detector and Pattern Generator as a master/slave system, see page 4-52.
2. Set the Synthesized Sweeper to the minimum module frequency and 0 dBm.

3. Connect the equipment as shown:



Note

Use only cables from the HP 15680A RF Accessory Kit to connect the Pattern Generator to the Error Detector. These cables are of equal length and type and have optimum characteristics for the following tests.

4. Press `select pattern` then use `more 1 of 3` to display `more 3 of 3` then press 2^7 `MARKDEN`.
5. Ensure that the Error Detector *CLK LOSS*, *DATA LOSS*, *SYNC LOSS* or *ERRORS* alarm indicators are not lit. Also check that the `Clock Loss`, `Data Loss`, `Sync Loss` or `Errors` alarm messages are not on the display.

Setting the 0/1 Threshold Manually

Note

The Error Detector sync time increases with longer patterns (higher numbers). The manual 0/1 threshold should always be set on the shortest pattern (2^7). Sync time on this pattern will be <2 seconds.

6. Press `data input` then set `0/1 THR AUTOMAN` to `MAN`.
7. Press `0/1 THRSHLD` then set the threshold to `1.00 V` using the numeric keys.
8. Check that there are Sync Loss and Errors alarms.
9. Decrease the threshold voltage using the rotating knob until the Sync Loss and Errors alarms disappear. Note the voltage ($V1$) at which this occurs.
10. Continue to decrease the threshold voltage until the Sync Loss and Errors alarms occur again. Note the voltage ($V2$) at which this occurs.
11. Calculate $(V1+V2)/2$ then use the numeric keys to enter this value as the new threshold voltage. There must be no Sync Loss and Errors alarms.

Single Errors with Variable Mark Density

12. Press select pattern then use more 1 of 3 to display more 3 of 3 then select MARK DENSITY followed by 1/8 , finally press EXIT .
13. Press gating then select MANUAL UNTIMED .
14. Press RUN GATING .
15. Select err-add , more 1 of 2 , error add then press ERR-ADD SINGLE once.
16. Ensure that the displayed Error Count is 1.
17. Check that the Error Count increments by 1 count each time ERR-ADD SINGLE is pressed. The Errors alarm message and indicator should flash momentarily each time an error is added.
18. Select gating then press STOP GATING , RUN GATING and STOP GATING in sequence to reset the error count to zero.
19. Repeat steps 12 to 18 with the MARK DENSITY set to 1/4 , 3/4 and 7/8 respectively.
20. Repeat steps 12 to 19 with select pattern set to 2^{10} MARKDEN , 2^{11} MARKDEN and 2^{13} MARKDEN respectively.

Note Do not press RUN GATING until resync has occurred (up to 30 seconds).

21. Return the pattern to 2^7 MARKDEN .
22. Repeat steps 12 to 21 with the Synthesized Sweeper set to the maximum module frequency.

Note If a Sync Loss alarms occurs at this frequency, select data input then press CLKEDGE NEG . Wait for resync to occur - ensure all alarms are off.

PRBS 2^n with Zero Substitution

Specifications

Zero Substitution Test Patterns:

2^{13}, polynomial $D^{13}+D^{12}+1=0$
2^{11}, polynomial $D^{11}+D^{9}+1=0$
2^{10}, polynomial $D^{10}+D^{7}+1=0$
2^{7}, polynomial $D^{7}+D^{6}+1=0$

In the above patterns an extra zero is added to extend the longest run of zeros by one.

Zeros can be substituted for data to extend the longest run of zeros in the above patterns. The longest run can be extended to the pattern length, minus one. The bit after the substituted zeros is set to 1.

Description

This test ensures that the Error Detector can synchronize to a 2^7, 2^{10}, $2^{11}$and 2^{13} pattern with extended runs of zeros.

A Pattern Generator is set to transmit each pattern - the Error Detector is monitored to ensure correct alignment across the full frequency range. The active clock edge on the Error Detector is inverted as required to achieve this.

The Error Detector Threshold (the level at which 0 to 1 transition occurs) is then adjusted manually to optimize the transition point for the chosen transmit level. Zeros can now be substituted into the pattern by increasing the *longest run of zeros* from minimum to maximum and verifying Error Detector alignment at selected *longest run of zeros*. This last step is repeated at each PRBS and at three discrete frequencies.

Equipment

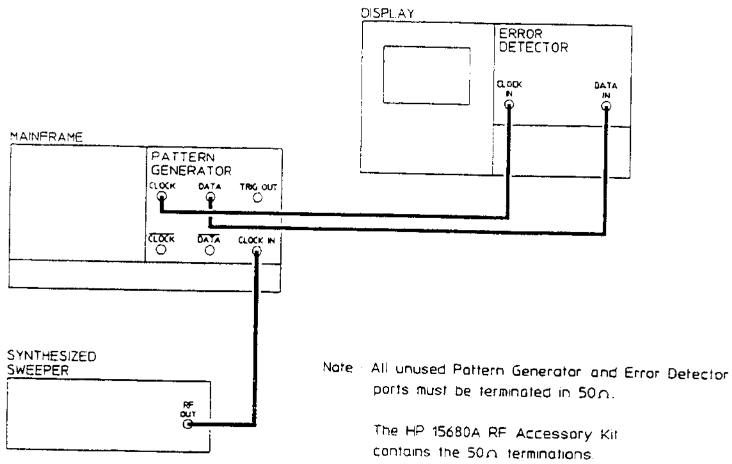
Synthesized Sweeper	: HP 83620A
RF Accessory Kit	: HP 15680A
Pattern Generator	: HP 70841A/B
Display	: HP 70004A

Procedure

Pattern Alignment

1. Initialize the Error Detector and Pattern Generator as a master/slave system, see page 4-52.
2. Set the Synthesized Sweeper to the minimum module frequency and 0 dBm.

3. Connect the equipment as shown:



Note

Use only cables from the HP 15680A RF Accessory Kit to connect the Pattern Generator to the Error Detector. These cables are of equal length and type and have optimum characteristics for the following tests.

4. Press `select pattern` then press `more 1 of 3` to display `more 2 of 3` then select 2^7 `ZEROSUB`.
5. Ensure that the Error Detector *CLK LOSS*, *DATA LOSS*, *SYNC LOSS* or *ERRORS* alarm indicators are not lit. Also check that the `Clock Loss`, `Data Loss`, `Sync Loss` or `Errors` alarm messages are not on the display.

Fixed Zero Substitution Alignment

6. Press `data input` followed by `CLK-DAT ALIGN` and wait for Clock to Data alignment to complete.
7. Press `select pattern` then use `more 1 of 3` to display `more 2 of 3` then select 2^7 `ZEROSUB`.

8. Select **LONGEST RUNZERO** then select the values listed in the following table using the numeric keys. Ensure that synchronization occurs within the resync time given in the table. There should be no Clock Loss, Sync Loss, Data Loss or Errors alarms after alignment has occurred. Return the **LONGEST RUN ZERO** to its lowest value when complete.

Pattern	Longest Run of Zeros	Resync Time
2^7 ZEROSUB	7, 20, 40, 60, 80, 84, 89,90	<2.0 s
2^{10} ZEROSUB	10, 200, 400, 600, 750, 794, 795	<2.0 s
2^{11} ZEROSUB	11, 400, 800, 1200, 1550, 1599, 1600	<2.0 s
2^{13} ZEROSUB	13, 2400, 5600, 6398, 6400	<2.0 s

9. Repeat steps 4 to 8 with the Synthesizer set to the maximum module frequency.

Internal User Selectable Pattern Synchronization and Error Detect

Specifications

Variable Length User Test Patterns (RAM stored)

Length: 1 to 4,194,304 bits

Resolution:
1 bit to 32,768 bits in 1 bit steps
32,768 to 65,536 bits in 2 bit steps
65,536 to 131,072 bits in 4 bit steps
131,072 to 262,144 bits in 8 bit steps
262,144 to 524,288 bits in 16 bit steps
524,288 to 1,048,576 bits in 32 bit steps
1,048,576 to 2,097,152 bits in 64 bit steps
2,097,152 to 4,194,304 bits in 128 bit steps

Four internal RAM stores are provided for user patterns. Each store can hold one pattern up 4,194,304 bits long.

Error Measurements

The error detector counts bit errors by comparing the incoming data bit-by-bit with the internally-generated reference pattern. All measurements run during the gating periods as described with the exception of Delta Error Count and Delta Error Ratio. These measurements run continuously to facilitate user adjustments for minimizing errors.

Error Count: The total number of errors during the gating period.

Delta Error Count: The number of errors in successive decisecond intervals.

Error Ratio: The ratio of counted errors to the number of bits in the selected gating period.

Delta Error Ratio: The ratio of counted errors to the number of bits in successive decisecond intervals.

Errored Intervals: Time intervals during which one or more errors occurred. These intervals are errored seconds, deciseconds, centiseconds or milliseconds.

Error Free Intervals: Time intervals of seconds, deciseconds, centiseconds or milliseconds, during which no errors occurred.

Description

This test ensures that the Error Detector can synchronize to and detect single and fixed errors in RAM stored *User Selectable Patterns*. The test patterns chosen will provide worst case alignment conditions for the Error Detector circuitry.

A Pattern Generator is set to transmit each of four preset patterns - the Error Detector is monitored to ensure correct alignment across the full frequency range. The active clock edge on the Error Detector is inverted as required to achieve this.

Single errors are then added to each transmitted pattern - the Error Detector is checked to ensure these errors are detected. The Pattern Generator is next set to its fixed error rate of $1x10^{-6}$ - the Error Detector is checked for the correct error rate and result analysis. Single and fixed error rates are verified at three discrete frequencies.

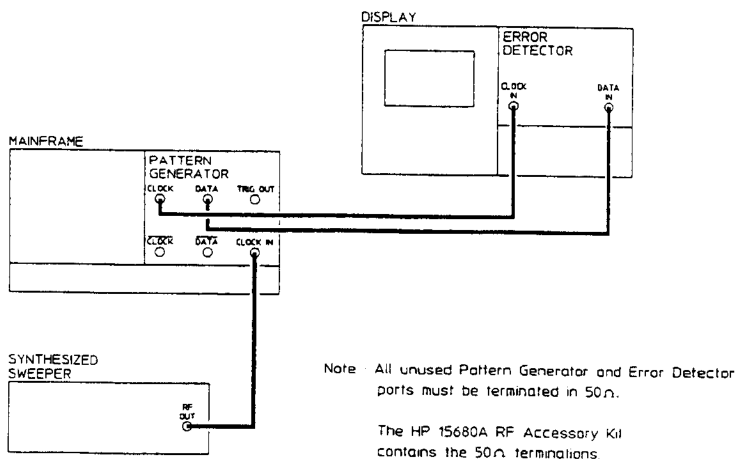
Equipment

Synthesized Sweeper : HP 83620A
RF Accessory Kit : HP 15680A
Pattern Generator : HP 70841A/B
Display : HP 70004A

Procedure

Pattern Alignment

1. Initialize the Error Detector and Pattern Generator as a master/slave system, see page 4-52.
2. Set the Synthesized Sweeper to the minimum module frequency and 0 dBm.
3. Connect the equipment as shown:



Note

Use only cables from the RF Accessory Kit to connect the Pattern Generator to the Error Detector. These cables are of equal length and type and have optimum characteristics for the following tests.

4. Press `more 1 of 2` followed by `edit usr-pat` then set up the user patterns as listed in the following table (see *Appendix B*).

`INTERNL PATT 1`	1001 0111 0010 110 (pattern length 15 bits)
`INTERNL PATT 2`	1111 1111 1111 1110 1111 1111 1111 1111 0000 0000 0000 0001 0000 0000 0000 0000 (pattern length 64 bits)
`INTERNL PATT 3`	1010 (repeat for pattern length of 255 bits)
`INTERNL PATT 4`	10 (pattern length of 2 bits)

5. Press `more 2 of 2` on the left of the display then press `select pattern`. Press `user pattern` twice then select `INTERNL PATT 1` to make Pattern 1 active.

6. Ensure that the Error Detector *CLK LOSS*, *DATA LOSS*, *SYNC LOSS* or *ERRORS* alarm indicators are not lit. Also check that the `Clock Loss`, `Data Loss`, `Sync Loss` or `Errors` alarm messages are not on the display. The error count should be 0.
7. Sweep the Synthesized Sweeper slowly between the minimum and maximum module frequencies and monitor the module and display for clock loss, data loss, sync loss or errors alarms. If a sync loss or errors alarm occurs at any frequency, select `data input`, then press `CLKEDGE NEG`. Check for pattern re-alignment, no alarm message on the display and no module alarm indicators.
8. Return the Synthesized Sweeper to the minimum module frequency.

Single Error Add

9. Select `gating` then press `MANUAL UNTIMED`.
10. Select `RUN GATING`.
11. Select `err-add`, `more 1 of 2`, `error add` then press `ERR-ADD SINGLE` once.
12. Ensure that the displayed `Error Count` is 1.
13. Check that the `Error Count` increments by 1 count each time `ERR-ADD SINGLE` is pressed. The `Errors` alarm message and indicator should flash momentarily each time an error is added.
14. Select `gating` then press `STOP GATING`, `RUN GATING` then `STOP GATING` in sequence to reset the error count to zero.
15. Repeat steps 10 to 14 with the synthesized Sweeper set to the maximum module frequency. If a Sync Loss alarm occurs at this frequency then press `data input` followed by `CLKEDGE NEG`.
16. Return the Synthesized Sweeper to the minimum module frequency.
17. Repeat steps 5 to 16 with `INTERNL PATT 2`, `INTERNL PATT 3` and `INTERNL PATT 4` as the active pattern.

Data Input Range (Automatic 0/1 Threshold)

Specifications

Data Sampling Clock Edge: Selectable rising or falling edge.

Termination Voltage: Selectable 0 V or −2 V nominal.

Level: Min, 0.5 V p-p; Max, 2.0 V p-p nominal.

Offset (nominal):

	Termination	
	50Ω to 0 V	**50Ω to −2 V**
Maximum Input Voltage	+1 V	0 V
Minimum Input Voltage	−3 V	−3 V

0/1 Threshold: The electrical interface allows for a range of input amplitudes and dc offsets. The 0/1 threshold is set using one of three modes:

Automatic Track: Tracks the mean dc level of the input signal. The measured threshold is displayed.

Automatic Center: The Error Detector sets the 0/1 threshold midway between two points, top and bottom of the *eye* where the bit error ratio is equal to the selectable threshold. The *eye* height is calculated and displayed.

Manual: Sets the 0/1 threshold manually.
Range - +1 to −3 V nominal.
Resolution - 1 mV nominal.

Description

This test ensures that the Error Detector can synchronize to a pattern with amplitude and offset within the range specified for the Error Detector Data Input.

A Pattern Generator is used to transmit the required levels and offsets. The minimum specified level is first verified on an Oscilloscope with a 1100 1100 User Pattern - the Error Detector is monitored to ensure correct alignment across the full frequency spectrum with this minimum level. The Pattern Generator is set to transmit $2^{23}-1$ PRBS with Data amplitude and offset (data Hi level) set to tabulated values. - the Error Detector is monitored to ensure correct alignment across the full frequency spectrum in each case. The pattern is chosen to satisfy requirements on synchronization and mark:space density.

Data Input Range (Automatic 0/1 Threshold)

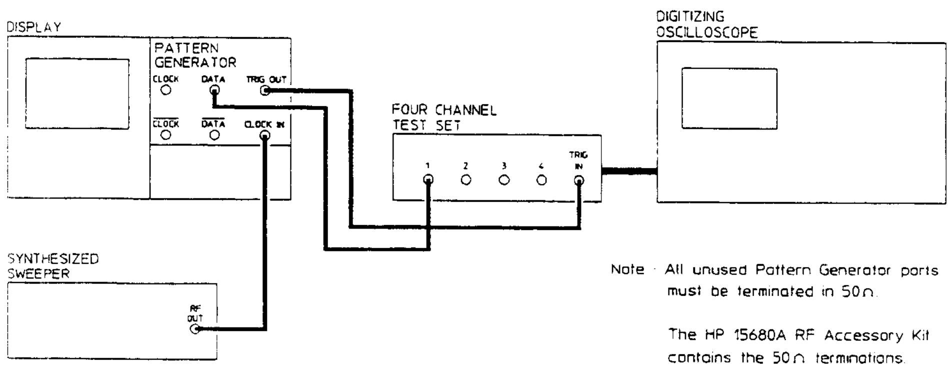
Equipment

Synthesized Sweeper	: HP 83620A
RF Accessory Kit	: HP 15680A
Digitizing Oscilloscope	: HP 54121T
Four Channel Test Set	: HP 54121A
Pattern Generator	: HP 70841A/B
Display	: HP 70004A

Procedure

Pattern Alignment with Minimum Data Amplitude

1. Initialize the Error Detector and Pattern Generator as a master/slave system, see page 4-52.
2. Set the Synthesized Sweeper to the minimum module frequency and 0 dBm.
3. Connect the equipment as shown;



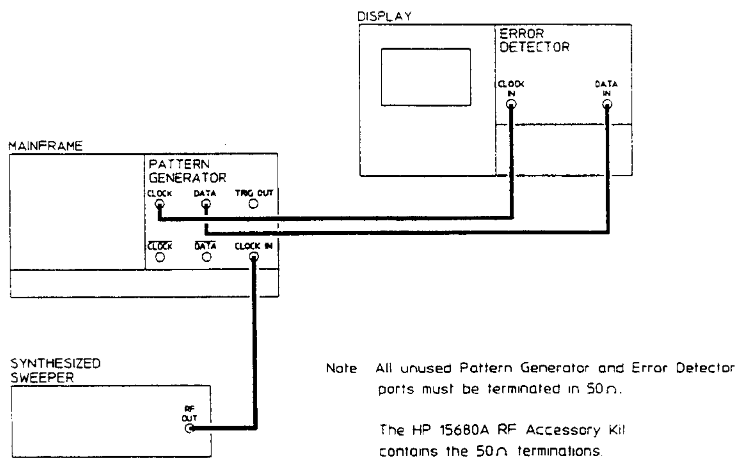
4. Set the Digitizing Oscilloscope for the following parameters:

CHAN	: Atten X1; CH1 on; CH2,3,4 off; CH 1 Amplitude 100 mV/Div; Offset 750 mV.
TIMEBASE	: Timebase 5 ns/Div; Delay 16 ns; Delay ref left ; Triggered
TRIGGER	: Trig Level −500 mV; Slope +ve; Atten X1; HF Sense off; HF Reject off
DISPLAY	: Display Mode Averaged; Number of Averages 8; Screen Single Bandwith 20 GHz.

Note The above parameters may be obtained by using the Digitizing Oscilloscope *Autoscale* function and modifying as required.

5. Press `more 1 of 2` followed by `edit usr-pat`. Select `PATTERN 1` then set it to 1100 1100 (see *Appendix B*).

6. Press more 2 of 2 on the left of the display followed by select pattern and INTERNL PATT 1 .
7. Press dat o/p followed by DATA AMPTD . Set the amplitude to 0.5 V using the numeric keys. Press DATA HI-LEVEL . Set the Hi level to 1.0 V using the numeric keys.
8. Adjust the Digitizing Oscilloscope delay to position the data pulse at the center of the display.
9. Use the Digitizing Oscilloscope MEASUREMENT function to measure the amplitude of the data pulse. If necessary adjust the Pattern Generator DATA AMPLTD until the amplitude of the data pulse is measured at 0.5 V.
10. Disconnect the oscilloscope and connect the equipment as shown:



Note Use only cables from the RF Accessory Kit to connect the Pattern Generator to the Error Detector. These cables are of equal length and type and have optimum characteristics for the following tests.

11. Ensure that the Error Detector *CLK LOSS*, *DATA LOSS*, *SYNC LOSS* or *ERRORS* alarm indicators are not lit. Also check that the Clock Loss , Data Loss , Sync Loss or Errors alarm messages are not on the display.
12. Sweep the Synthesized Sweeper slowly between the minimum and maximum module frequencies and monitor the module and display for clock loss, data loss, sync loss or errors alarms.

    If a sync loss or errors alarm occurs at any frequency, select data input , then press CLKEDGE NEG . Check for pattern re-alignment, no alarm message on the display and no module alarm indicators.
13. Repeat step 12 with the Error Detector terminated in −2 V (press data input followed by TERM −2 V).
14. Return the Error Detector termination to 0 V.

Pattern Alignment with Selected Data Amplitude and Offset (0 V Term)

15. Press select pattern then set the pattern to $2^{23}-1$.

16. Repeat step 12 with the Pattern Generator DATA AMPLTD and DATA HI LEVEL set to the values shown in the table below. (Verify the Data Amplitude on the Digitizing Oscilloscope.)

DATA AMPLITUDE	DATA HI LEVEL
500 mV	1.0 V
500 mV	−2.5 V
*2.0 V	1.0 V
2.0 V	−1.0 V

*Set DATA HI-LEVEL before DATA AMPLTD .

17. Return the DATA AMPLTD to 0.5 V and the DATA HI-LEVEL to 1 V.

Pattern Alignment with Selected Data Amplitude and Offset (−2 V Term)

18. Press data input followed by TERM −2 V.

19. Press dat o/p followed by more 1 of 2 on the right of the display.

20. Select TERM −2 V.

21. Repeat step 12 with the Pattern Generator DATA AMPLTD and DATA HI-LEVEL set to the values shown in the table below:

DATA AMPLITUDE	DATA HI LEVEL
500 mV	0 V
500 mV	−2.5 V
*2.0 V	0 V
2.0 V	−1.0 V

*Set DATA HI-LEVEL before DATA AMPLTD .

Error Output Waveform and Data Input Delay

Specifications

Error Output

Provides an electrical signal to indicate received errors. The error output pulse is the logical *OR* of all errors in a 16-bit period.

All specifications are for the output terminated 50Ω to 0V.

Format: RZ, active high.

Amplitude: High: 0 V nominal. Low: −800 mV nominal.

Pulse Width: For 1-bit error: 8 clock pulses nominal.

Impedance: 50Ω nominal.

Interface: dc coupled.

Connector: BNC female.

Data Input Delay

The data sampling point can be set automatically to the center of the *eye*. The error detector sets the data/clock delay midway between two points either side of the *eye* where the bit error ratio is equal to a selectable threshold. The *eye* width is calculated and displayed. The sampling point can also be set manually by altering the data/clock delay.

Data delay variation vs selected clock edge:
Range: ±1 ns nominal.
Resolution: 1 ps nominal.
Automatic Data/Clock Alignment and 0/1 Threshold Center: Selectable error-ratio thresholds from 0 to 1 x 10^1.

Return Loss: 300 kHz to maximum operating frequency > 15 dB typical.

Impedance: 50Ω nominal.

Interface: dc coupled.

Connector: N-type female.

Description

The rear panel Error Output signal is verified by checking waveform parameters on a Digitizing Oscilloscope with Data Error Rate of 3.125e-02 (one error in every 32 bits). This Rate is obtained by independently setting the Pattern Generator and Error Detector to the same User Selectable Word pattern (pattern length is 32 bits), except that the last bit in the Pattern Generator word is inverted. The Error Detector will align to this pattern (with an error rate of one in 32) as the default alignment threshold is one error in every 10 bits.

The *User Selectable Words* can only be independently set if the Pattern Generator and Error Detector are configured as a *Master/Master* system (see page 4-53).

The data input delay is typically ±1 ns with respect to the clock signal. A 500 MHz clock signal is use to verify the delay operation. The delay is varied and at some point within the ±1 ns delay range Sync Loss must occur (due to the clock period being 2 ns).

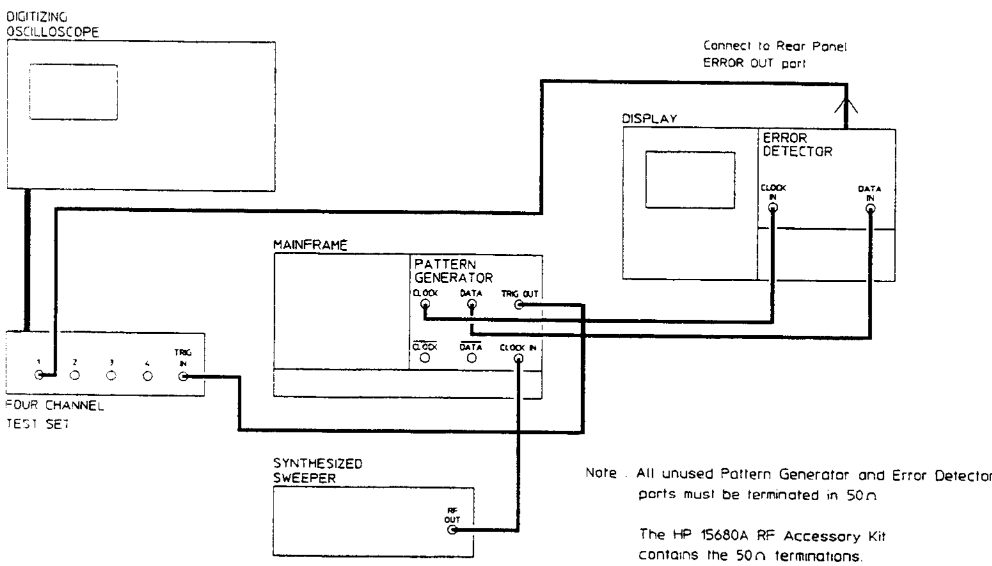
Equipment

Synthesized Sweeper : HP 83620A
RF Accessory Kit : HP 15680A
Digitizing Oscilloscope : HP 54121T
Four Channel Test Set : HP 54121A
Pattern Generator : HP 70841A/B
Display : HP 70004A

Procedure

Pattern Alignment in Master-Master

1. Initialize the Error Detector and Pattern Generator as a master/master system, see page 4-53.
2. Set the Synthesized Sweeper to the maximum module frequency and 0 dBm.
3. Connect the equipment as shown:



Note Use only cables from the RF Accessory Kit to connect the Pattern Generator to the Error Detector. These cables are of equal length and type and have optimum characteristics for the following tests.

4. Ensure that the Error Detector *CLK LOSS*, *DATA LOSS*, *SYNC LOSS* or *ERRORS* alarm indicators are not lit. Also check that the `Clock Loss`, `Data Loss`, `Sync Loss` or `Errors` alarm messages are not on the display. If alarms are present, press `data input` on the Error Detector display followed by `CLKEDGE NEG`. Ensure the alarms disappear.
5. Press `DISPLAY` followed by `NEXT INST` to show the Pattern Generator parameters on the display then press `USER`.

6. Press `edit-usr-pat` then `INTERNL PATT 1`. Set the user pattern to 1010 1010 1010 1010 1010 1010 1010 1010 (32 bits) - see *Appendix B*.
7. Press `select pattern` followed by `user pattern`. Press `user pattern` again then select `INTERNL PATT 1`.
8. Press (DISPLAY) followed by (NEXT INST) to show the Error Detector parameters on the display then press (USER).
9. Repeat steps 6 and 7 for the Error Detector module.
10. Ensure that the Error Detector *CLK LOSS*, *DATA LOSS*, *SYNC LOSS* or *ERRORS* alarm indicators are not lit. Also check that the `Clock Loss`, `Data Loss`, `Sync Loss` or `Errors` alarm messages are not on the display.
11. Set the Error Detector user pattern to 1010 1010 1010 1010 1010 1010 1010 1011 (last bit inverted).
12. Ensure that the `Errors` alarm message is displayed and that the *ERRORS* alarm indicator is lit.

Fixed Error Rate Count

13. Press `gating` then select `SINGLE`. Set `GATING PERIOD` to 10 seconds using the numeric keys.
14. Press `RUN GATING`.
15. Wait for gating to finish then note the *Error Ratio* reading on the display. This will be typically 3.125e-02.

Measuring Error Output Waveform Parameters

16. Set the Digitizing Oscilloscope as follows:

CHAN	: Atten X1; CH1 on; CH2,3,4 off; CH 1 Amplitude 200 mV/Div; Offset −400 mV
TIMEBASE	: Timebase 1 ns/Div; Delay 16 ns; Delay ref left ; Triggered
TRIGGER	: Trig Level −500 mV; Slope +ve; Atten X1; HF Sense off; HF Reject off
DISPLAY	: Display Mode Averaged; Number of Averages 8; Screen Single Bandwith 20 GHz.

Note

The above parameters may be obtained by using the Digitizing Oscilloscope *Autoscale* function and modifying as required.

17. Adjust the Digitizing Oscilloscope delay and timebase to center one Error pulse across the display.
18. Measure the amplitude and width of the displayed pulse. *Typical* amplitude will be −0.80 V (that is, Hi level is 0 V, Low level is −0.80 V) and *typical* width (measured at mid-amplitude) will be 2.67 ns.

Data Input Delay Check

19. Press `data input` followed by `DAT I/P DELAY`, then set the Pattern Generator delay to +1 ns using the numeric keys.
20. Set the Synthesized Sweeper to 500 MHz at 0 dBm. If a Sync Loss alarm occurs, press `CLKEDGE NEG` - ensure the alarm disappears.
21. Change the data input delay slowly to −1 ns using the rotary knob.
22. Check that Sync Loss occurs as the delay is reduced then is regained as the delay is further reduced.

Data Input Invert

Specifications

Data Polarity: Selectable normal or inverted.

Description

The Error Detector input data can be normal or inverted. The inverted input is tested by setting the transmitted User Word to be the inverse of the received User Word and ensuring that these patterns sync up with no errors across the full frequency range.

The *User Selectable Words* can only be independently set if the Pattern Generator and Error Detector are configured as a *Master/Master* system (see page 4-53).

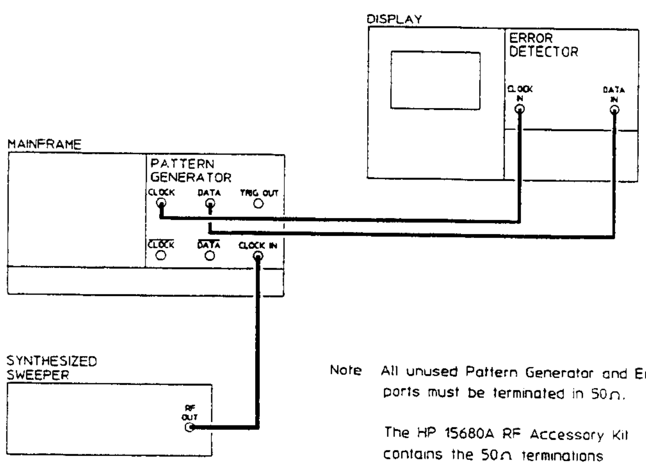
Equipment

Synthesized Sweeper	: HP 83620A
RF Accessory Kit	: HP 15680A
Digitizing Oscilloscope	: HP 54121T
Four Channel Test Set	: HP 54121A
Pattern Generator	: HP 70841A/B
Display	: HP 70004A

Procedure

Pattern Alignment in Master-Master

1. Initialize the Error Detector and Pattern Generator as a master/master system, see page 4-53.
2. Set the Synthesized Sweeper to the minimum module frequency and 0 dBm.
3. Connect the equipment as shown:



Note All unused Pattern Generator and Error Detector ports must be terminated in 50Ω.

The HP 15680A RF Accessory Kit contains the 50Ω terminations.

Note

Use only cables from the RF Accessory Kit to connect the Pattern Generator to the Error Detector. These cables are of equal length and type and have optimum characteristics for the following tests.

4. Press (DISPLAY) followed by NEXT INST to show the Error Detector parameters on the display then press (USER).
5. Ensure that the Error Detector *CLK LOSS*, *DATA LOSS*, *SYNC LOSS* or *ERRORS* alarm indicators are not lit. Also check that the Clock Loss , Data Loss , Sync Loss or Errors alarm messages are not on the display.
6. Press data input then set 0/I THR AUTOMAN to MAN (manual threshold).
7. Press edit-usr-pat then PATTERN 1 . Set pattern 1 to 1000 0000 0000 0000 (16 bits) - see *Appendix B*
8. Press select pattern followed by user pattern . Press user pattern again then select USER PATTN 1 .
9. Press (DISPLAY) followed by (NEXT INST) to show the Error Detector parameters on the display then press (USER).
10. Repeat steps 7 and 8 for the Pattern Generator module.
11. Ensure that the Error Detector *CLK LOSS*, *DATA LOSS*, *SYNC LOSS* or *ERRORS* alarm indicators are not lit.

Pattern Alignment with Data Output and Data Input Inverted

12. Press dat o/p and set POLRITY NORMINV to INV (inverted).
13. Press (DISPLAY) followed by (NEXT INST) to show the Error Detector parameters on the display then press (USER).
14. Press data input and set POLRITY NORMINV to INV (inverted).
15. Ensure that the Error Detector *CLK LOSS*, *DATA LOSS*, *SYNC LOSS* or *ERRORS* alarm indicators are not lit. Also check that the Clock Loss , Data Loss , Sync Loss or Errors alarm messages are not on the display.

Pattern Alignment with Data Output Inverted

16. Press data input and set POLRITY NORMINV to NORM (normal).
17. Ensure that the Error Detector *SYNC LOSS* and *ERRORS* alarm indicators are lit. Also check that the Sync Loss and Errors alarm messages are on the display.
18. Press edit-usr-pat then PATTERN 1 .
19. Set Pattern 1 to 0111 1111 1111 1111 (16 bits)

20. Ensure that the Error Detector *CLK LOSS*, *DATA LOSS*, *SYNC LOSS* or *ERRORS* alarm indicators are not lit. Also check that the `Clock Loss` , `Data Loss` , `Sync Loss` or `Errors` alarm messages are not on the display.

Pattern Alignment with Data Input Inverted

21. Press `data input` and set `POLRITY NORMINV` to `INV` .
22. Ensure that the Error detector *SYNC LOSS* and *ERRORS* alarm indicators are lit. Also check that the `Sync Loss` and `Errors` alarm messages are on the display.
23. Press (DISPLAY) followed by (NEXT INST) to show the Pattern Generator parameters on the display then press (USER).
24. Press `dat o/p` and set `POLRITY NORMINV` to `NORM`
25. Press (DISPLAY) followed by (NEXT INST) to show the Error detector parameters on the display.
26. Ensure that the Error Detector *CLK LOSS*, *DATA LOSS*, *SYNC LOSS* or *ERRORS* alarm indicators are not lit. Also check that the `Clock Loss` , `Data Loss` , `Sync Loss` or `Errors` alarm messages are not on the display.

Pattern Synchronization Threshold

Specifications

Synchronization to the incoming pattern can be performed automatically or manually. In manual mode, the Sync Start key forces the Error Detector to attempt synchronization with the received pattern.

Sync Gain/Loss Criteria: The criterion for gaining or losing synchronization is the error ratio in a 1 ms interval. Selectable error-ratio thresholds of 1 x 10^{-1}, 10^{-2}, 10^{-3} , 10^{-4}, 10^{-5}, 10^{-6}, 10^{-7} and 10^{-8} are provided.

Resync Time: (Under error free conditions) PRBS $2^{31}-1$, $2^{23}-1$, $2^{15}-1$: $<$ 200 ms nominal; PRBS $2^{10}-1$, $2^{7}-1$ $<$ 500 ms nominal.
User Patterns <10 kbit/s: <2 s STM16 Frame PRBS data @ 2.5 GHz: <5 s.

Description

The Error Detector Pattern synchronization threshold is the error rate (measured in a 1 ms interval) above which the Error Detector is defined to have lost synchronization with the incoming pattern. Four of the user selectable sync thresholds are tested in both automatic and manual mode.

In automatic sync mode the Error Detector will begin to synchronize to the pattern immediately the error rate falls below the threshold. This is tested by transmitting a pattern with error rate above the threshold and checking that the Error Detector does not synchronize. With the error rate set below the threshold the Error Detector should now automatically synchronize to the incoming pattern and count the correct number of errors. With manual sync mode selected, synchronization will only occur once the operator has initiated it from the front panel keyboard. This is tested in 1e−02 sync threshold only. All tests are performed at maximum bit rate (clock frequency).

Because only one error add rate is available from the HP 70841B Pattern Generator, the error rates required to test synchronization thresholds can only be obtained by transmitting and receiving non-identical *user selectable patterns*. This is done by inverting 1 in every X bits in the transmitted pattern - where $1/X <$ or $>$ the sync threshold under test.

The *User Selectable Patterns* can only be independently set if the Pattern Generator and Error Detector are configured as a *Master/Master* system.

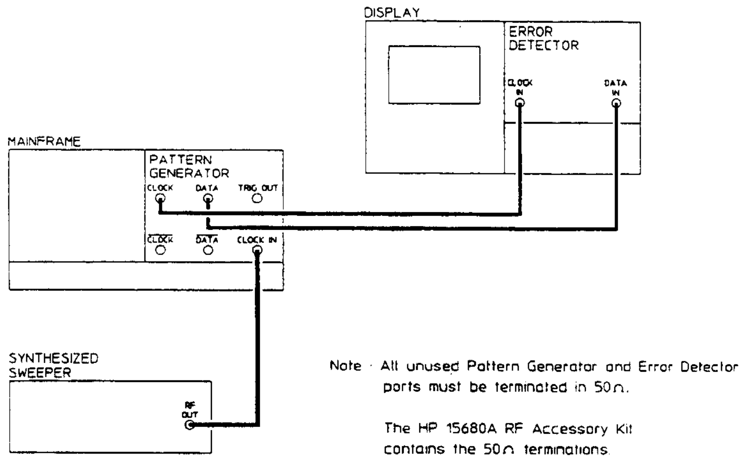
Equipment

Synthesized Sweeper	: HP 83620A
RF Accessory Kit	: HP 15680A
Pattern Generator	: HP 70841A/B
Display	: HP 70004A

Procedure

Pattern Alignment in Master/Master mode

1. Initialize the Error Detector and Pattern Generator as a master/master system, see page 4-53.
2. Set the Synthesized Sweeper to maximum module frequency and 0 dBm.
3. Connect the equipment as shown:



Note

Use only cables from the RF Accessory Kit to connect the Pattern Generator to the Error Detector. These cables are of equal length and type and have optimum characteristics for the following tests.

4. Press `data input` then `more 1 of 2`. Press `CLK-DAT ALIGN` and wait for clock to Data alignment to complete.
5. The Error Detector *CLK LOSS*, *DATA LOSS*, *SYNC LOSS* or *ERRORS* alarm indicators should not be lit. The `Clock Loss`, `Data Loss`, `Sync Loss` or `Errors` alarm messages should not be on the display.
6. Press `edit usr-pat` on the Pattern Generator display and set `INTERNL PATT 4` to 1010 (4 bits) - see *Appendix B*.
7. Press `select pattern` followed by `user pattern`. Press `user pattern` again then select `INTERNL PATT 4`.
8. Press (DISPLAY) followed by `NEXT INST` and (USER) to show the Error Detector on the display.
9. Repeat steps 6 and 7 with the Error Detector `INTERNL PATT 4` set to 1010 1010 1010 1010 1010 1010 1010 1010 1010 1010 10 (42 bits).
10. Ensure that the Error Detector *CLK LOSS*, *DATA LOSS*, *SYNC LOSS* or *ERRORS* alarm indicators are not lit. Also check that the `Clock Loss`, `Data Loss`, `Sync Loss` or `Errors` alarm messages are not on the display.

Checking for Sync Loss with 1e-01 Threshold

11. Set the Error Detector Sync Threshold to 1e-01 by pressing More 1 of 2 followed by sync, SYNC THRSHLD and (1e−01).
12. Return to edit usr-pat and set the Error Detector INTERNL PATT 4 to 1010 1010 1010 1010 1010 1010 1010 1010 1010 0101 00 (42 bits). This gives an error ratio of 1.19e−01 (5 bits in 42) which is above the sync threshold.
13. Ensure that the Errors and Sync Loss alarm messages are displayed and the *ERRORS* and *SYNC LOSS* alarm indicators are lit.
14. Set the Error Detector INTERNL PATT 4 to 1010 1010 1010 1010 1010 1010 1010 1010 1010 0101 10 (42 bits). This gives an error ratio of 0.95e−01 (4 bits in 42)which is below the sync threshold.
15. The Sync Loss alarm message should no longer be displayed and the *SYNC LOSS* alarm indicator should no longer be lit.

Checking Error Ratio with Patterns in Sync

16. Press the Error Detector select page then press MAIN RESULTS to show *Error Count, Delta Error Count, Error Ratio* and *Delta Error Ratio*.
17. Press gating then select SINGLE followed by GATING PERIOD. Set the gating period to 10 seconds using the numeric keys.
18. Press RUN GATING - ensure the Error Detector gating indicator is lit.
19. Wait for gating to finish (gating indicator not lit) then note the *Error Ratio* reading on the display - typically 9.5e−02.

Checking for Sync Loss with 1e-02 Threshold

20. Press More 1 of 2 followed by sync and SYNC THRSHLD. Set the Error Detector sync threshold to 1e−02.
21. Press (DISPLAY) followed by NEXT INST and (USER) to show the Pattern Generator.
22. Press edit usr-pat followed by INTERNL PATT 4.
23. Press load block followed by 2^7PRBS and NO MODIFY.
24. Reduce the pattern length to 99 bits by selecting SET PATTERN LENGTH then setting the length to 99 bits.
25. Repeat the previous four steps on the Error Detector display.
26. Ensure that the Error Detector *CLK LOSS*, *DATA LOSS*, *SYNC LOSS* and *ERRORS* alarm indicators are not lit. Also check that the Clock Loss, Data Loss, Sync Loss and Errors alarm messages are not on the display.

27. Invert the first bit of the Error Detector `INTERNL PATT 4`. This gives an error ratio of 1.01e−02 (1 bit in 99) which is above the threshold.
28. Ensure that the `Errors` and `Sync Loss` alarm messages are displayed and the *ERRORS* and *SYNC LOSS* alarm indicators are lit.

Checking Error Ratio with Patterns in Sync

29. Increase the `INTERNL PATT 4` length to 102 bits on both the Pattern Generator and Error Detector.
30. The `Sync Loss` alarm message should no longer be displayed and the *SYNC LOSS* alarm indicator should no longer be lit.
31. Press `gating` on the Error Detector display then press `RUN GATING`.
32. Wait for gating to finish then note the *Error Ratio* reading on the display - typically 9.804e-03.

Checking Manual Sync Mode

33. Set the Error Detector to manual sync mode by selecting `More 1 of 2` then press `sync`. Set `SYNC AUTOMAN` to `MAN` (manual).
34. Invert the second bit of `INTERNL PATT 4` pattern on the Error Detector.

    Return to `Edit User INTERNL PATT 4` on the Error Detector and invert the second bit of the pattern.
35. Ensure that the `Errors` and `Sync Loss` alarm messages are displayed and the *ERRORS* and *SYNC LOSS* alarm indicators are lit.
36. Invert the first two bits of `INTERNL PATT 4` on the Error Detector to return the pattern to its original format.
37. Ensure that the `Errors` and `Sync Loss` alarm messages are still displayed and the *ALARM* and *SYNC LOSS* alarm indicators are still lit.
38. Return to `sync` then press `SYNC START`.
39. The `Errors` and `Sync Loss` alarm messages should disappear. The *ERRORS* and *SYNC LOSS* alarm indicators should not be lit.
40. Return the Error Detector `SYNC AUTOMAN` setting to `AUTO` (automatic)

Checking for Sync Loss with 1e-03 Threshold

41. Set the Error Detector sync threshold to 1e-03.
42. Press (DISPLAY) followed by `NEXT INST` and (USER) to show the Pattern Generator.
43. Press `edit usr-pat` followed by `INTERNL PATT 4`.
44. Press `recall pattern` followed by 2^{10}`PRBS` and `NO MODIFY`.

45. Reduce the pattern length to 992 bits by selecting SET PATTERN LENGTH then setting the length to 992 bits.
46. Repeat the previous four steps on the Error Detector display.
47. Wait for resync to occur. Check that the Clock Loss , Data Loss , Sync Loss and Errors alarm messages are not on the display. Resync must occur within 2 seconds of completing *step 46*.
48. Invert the first bit of the Error Detector INTERNL PATT 4 . This gives an error ratio of 1.008e−03 (1 bit in 992) which is above the threshold.
49. Ensure that the Errors and Sync Loss alarm messages are displayed and the *ERRORS* and *SYNC LOSS* alarm indicators are lit.

Checking Error Ratio with Patterns in Sync

50. Increase INTERNL PATT 4 length to 1024 bits on both the Pattern Generator and Error Detector.
51. Wait for resync to occur then check that the Sync Loss alarm message is no longer displayed and the *SYNC LOSS* alarm indicator is no longer lit.
52. Press gating on the Error Detector then select RUN GATING .
53. Wait for gating to finish then note the *Error Ratio* reading on the display - typically 9.766e-04.

Checking for Sync Loss with 1e-04 Threshold

54. Set the Error Detector sync threshold to 1e-04.
55. Press (DISPLAY) followed by NEXT INST and (USER) to show the Pattern Generator.
56. Press edit usr-pat followed by INTERNL PATT 4 .
57. Press recall pattern followed by 2^{13}PRBS and NO MODIFY .
58. Repeat the previous three steps on the Error Detector display.
59. Wait for resync to occur. Check that the Clock Loss , Data Loss , Sync Loss and Errors alarm messages are not on the display. Resync must occur within 2 seconds of completing *step 58*.
60. Invert the first bit of the Error Detector INTERNL PATT 4 . This gives an error ratio of 1.22e−04 (1 bit in 8192) which is above the threshold.
61. Ensure that the errors and Sync Loss alarm messages are displayed and the *ERRORS* and *SYNC LOSS* alarm indicators are lit.

Disc Drive

The following test will ensure that the pattern generator disc drive is able to store and recover patterns without error. Both pattern generator and error detector are setup for 2^{13}PRBS user patterns from an internal pattern store. This pattern is first saved to a pre-formatted disc, then recovered. The recovered pattern is compared with the error detector pattern to ensure no errors have been introduced.

Procedure

1. Leave the equipment setup as for step 61 in the previous test.
2. Invert the first bit of the error detector **INTERNL PATT 4**.
3. Wait for resync to occur. When this happens the error detector CLK LOSS, DATA LOSS, SYNC LOSS and ERRORS alarm messages are not displayed, and alarm indicators are not lit.
4. Fit a formatted disc into the pattern generator disc drive (see Appendix B).
5. Press (DISPLAY) followed by **NEXT INSTR** to show the pattern generator display.
6. Press **edit usr-pat** followed by **INTERNL PATT 4** (2^{13}PRBS).
7. Press **save pattern** then **DISC PATT 5**. This saves the 2^{13}PRBS on disc. Note: The LED on the disc drive should light as the contents of INTERNL PATT 4 are written to it.
8. Press **select pattern** then **user pattern**. Press **DISC PATT 5** to recall the 2^{13}PRBS stored on disc.
9. Check that the error detector CLK LOSS, DATA LOSS, SYNC LOSS and ERRORS alarm indicators are not lit.

Hewlett-Packard	*Tested by:*
Model 71600B	*Date:*
Series System	*Serial No:*

Operational Verification Test Record

Page No.	Test Description		Result		
			Min	Actual	Max
	PATTERN GENERATOR				
	Clock Input Levels				
4-8	Step 9:	Waveform correct (√)			
	Step 11:	Waveform correct (√)			
	Step 12:	Clock Loss alarm present (√)			
4-9	Step 13:	Waveform correct and Clk Loss alarm present (√)			
	Clock Output Waveforms				
4-12	Step 7:	HP 70841A:			
		Rise Time - 10 to 90%			120 ps
		Fall Time - 10 to 90%			120 ps
		Preshoot			15%
		Overshoot			15%
4-13	Step 8:	HP 70841A:			
		Clock Ampl. 0.5 V:			
		Waveform correct (√)			
		Rise Time - 10 to 90%			120 ps
		Fall Time - 10 to 90%			120 ps
		Preshoot			15%
		Overshoot			15%
		Clock Ampl. 2 V:			
		Waveform correct (√)			
		Rise Time - 10 to 90%			120 ps
		Fall Time - 10 to 90%			120 ps
		Preshoot			15%
		Overshoot			15%

Operational Verification Test Record (continued)

Page No.	Test Description		Result		
			Min	Actual	Max
4-13	Step 11:	HP 70841A:			
		Clock Ampl. 2 V:			
		Waveform correct (√)			
		Rise Time - 10 to 90%			120 ps
		Fall Time - 10 to 90%			120 ps
		Preshoot			15%
		Overshoot			15%
		Clock Ampl. 1 V:			
		Waveform correct (√)			
		Rise Time - 10 to 90%			120 ps
		Fall Time - 10 to 90%			120 ps
		Preshoot			15%
		Overshoot			15%
		Clock Ampl. 0.5 V:			
		Waveform correct (√)			
		Rise Time - 10 to 90%			120 ps
		Fall Time - 10 to 90%			120 ps
		Preshoot			15%
		Overshoot			15%
4-13	Step 15:	HP 70841A:			
		Rise Time - 10 to 90%			1.3 ns
		Fall Time - 10 to 90%			1.3 ns
		Preshoot			15%
		Overshoot			15%
4-14	Step 16:	HP 70841A:			
		Clock Ampl. 0.5 V:			
		Waveform correct (√)			
		Rise Time - 10 to 90%			1.3 ns
		Fall Time - 10 to 90%			1.3 ns
		Preshoot			15%
		Overshoot			15%
		Clock Ampl. 2 V:			
		Waveform correct (√)			
		Rise Time - 10 to 90%			1.3 ns
		Fall Time - 10 to 90%			1.3 ns
		Preshoot			15%
		Overshoot			15%

Operational Verification Test Record (continued)

Page No.	Test Description		Result		
			Min	Actual	Max
4-14	Step 19:	HP 70841A:			
		Clock Ampl. 0.5 V:			
		Waveform correct (√)			
		Rise Time - 10 to 90%			1.3 ns
		Fall Time - 10 to 90%			1.3 ns
		Preshoot			15%
		Overshoot			15%
		Clock Ampl. 1 V:			
		Waveform correct (√)			
		Rise Time - 10 to 90%			1.3 ns
		Fall Time - 10 to 90%			1.3 ns
		Preshoot			15%
		Overshoot			15%
		Clock Ampl. 2 V:			
		Waveform correct (√)			
		Rise Time - 10 to 90%			1.3 ns
		Fall Time - 10 to 90%			1.3 ns
		Preshoot			15%
		Overshoot			15%
4-14	Step 22:	Waveforms 180° out-of-phase (√)			
4-15	Step 31:	Rising edge of pulse correct (√)			
	Data Output Waveforms				
4-19	Step 10:	HP 70841A:			
		Rise Time - 10 to 90%			120 ps
		Rise Time - 20 to 80%			90 ps
		Fall Time - 10 to 90%			120 ps
		Fall Time - 20 to 80%			90 ps
		Preshoot			15%
		Overshoot			15%

Operational Verification Test Record (continued)

Page No.	Test Description		Result		
			Min	Actual	Max
4-20	Step 12:	HP 70841A:			
		Rise Time - 10 to 90%			120 ps
		Rise Time - 20 to 80%			90 ps
		Fall Time - 10 to 90%			120 ps
		Fall Time - 20 to 80%			90 ps
		Preshoot			15%
		Overshoot			15%
4-20	Step 15:	HP 70841A:			
		Rise Time - 10 to 90%			120 ps
		Rise Time - 20 to 80%			90 ps
		Fall Time - 10 to 90%			120 ps
		Fall Time - 20 to 80%			90 ps
		Preshoot			15%
		Overshoot			15%
4-21	Step 19:	HP 70841A:			
		Rise Time - 10 to 90%			150 ps
		Fall Time - 10 to 90%			150 ps
		Preshoot			15%
		Overshoot			15%
4-21	Step 20:	HP 70841A:			
		Clock Ampl. 0.5 V:			
		Waveform correct (√)			
		Rise Time - 10 to 90%			150 ps
		Fall Time - 10 to 90%			150 ps
		Preshoot			15%
		Overshoot			15%
		Clock Ampl. 2 V:			
		Waveform correct (√)			
		Rise Time - 10 to 90%			150 ns
		Fall Time - 10 to 90%			150 ns
		Preshoot			15%
		Overshoot			15%

Operational Verification Test Record (continued)

Page No.	Test Description		Result		
			Min	Actual	Max
4-21	Step 23:	HP 70841A:			
		Clock Ampl. 0.5 V:			
		Waveform correct (√)			
		Rise Time - 10 to 90%			150 ps
		Fall Time - 10 to 90%			150 ps
		Preshoot			15%
		Overshoot			15%
		Clock Ampl. 2 V:			
		Waveform correct (√)			
		Rise Time - 10 to 90%			150 ps
		Fall Time - 10 to 90%			150 ps
		Preshoot			15%
		Overshoot			15%
4-21	Step 26:	Waveforms 180° out-of-phase (√)			
	PRBS 2^n-1 Pattern Length				
4-28	Step 5:	2^7-1	4095.9		4096.1
		$2^{10}-1$	32767.9		32768.1
		$2^{15}-1$	131071.9		131072.1
		$2^{23}-1$	33554431.9		33554432.1
4-28	Step 8:	2^7-1	16255.9		16256.1
		$2^{10}-1$	130943.9		130944.1
		$2^{15}-1$	524271.9		524272.1
		$2^{23}-1$	34217711.9		34217712.1
4-29	Step 9:	2^7-1	16255.9		16256.1
		$2^{10}-1$	130943.9		130944.1
		$2^{15}-1$	524271.9		524272.1
		$2^{23}-1$	34217711.9		34217712.1
	Step 17:	2^7-1	16255.9		16256.1

Operational Verification Test Record (continued)

Page No.	Test Description	Result		
		Min	Actual	Max
	ERROR DETECTOR			
	Clock Input Levels			
4-59	Step 7: No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
	Step 8: No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
	Step 10: Clk Loss alarm present (√)			
	Step 13: No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
	PRBS 2^n Pattern Synchronization, Error Detect and Memory Backup			
4-65	Step 5: No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
4-66	Step 7: No Clk Loss, Data Loss, Sync Loss or Errors alarms present with the following PRBS: 2^{10} MARKDEN (√) 2^{11} MARKDEN (√) 2^{13} MARKDEN (√)			
	Step 12: Error count is 1 (√)			
	Step 13: Error count increments by 1 and audible beep sounds each time the key is pressed (√)			

Operational Verification Test Record (continued)

Page No.	Test Description	Result		
		Min	Actual	Max
4-66	Step 15: Error count increments by 1 and audible beep sounds each time the key is pressed at the following PRBS: 2^{11} MARKDEN (√) 2^{10} MARKDEN (√) 2^{7} MARKDEN (√)			
	Step 16: Maximum module frequency: Error count increments by 1 and audible beep sounds each time the key is pressed at the following PRBS: 2^{7} MARKDEN (√) 2^{10} MARKDEN (√) 2^{11} MARKDEN (√) 2^{13} MARKDEN (√)			
	Step 20: Errors alarm present (√)			
4-67	Step 23: Typical error ratio correct (√) Typical delta error ratio correct (√)			
	Step 24: Typical error ratio and delta error ratio correct at the following PRBS: 2^{10} MARKDEN (√) 2^{11} MARKDEN (√) 2^{13} MARKDEN (√)			
	Step 26: Typical error ratio and delta error ratio correct at the following PRBS: 2^{7} MARKDEN (√) 2^{10} MARKDEN (√) 2^{11} MARKDEN (√) 2^{13} MARKDEN (√)			

Operational Verification Test Record (continued)

Page No.	Test Description		Result		
			Min	Actual	Max
4-67	Step 29:	Time/date correct (√)			
	Step 30:	Power Loss Second displayed (√)			
	Error Output Waveform and Data Input Delay				
4-82	Step 4:	No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
4-83	Step 10:	No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
	Step 12:	Errors alarm indicated and displayed (√)			
	Step 15:	Typical error ratio correct (√)			
4-84	Step 18:	Typical Pulse Amplitude correct (√)			
		Typical Pulse Width correct (√)			
	Step 22:	Sync lost and regained as delay is reduced (√)			

Hewlett-Packard Model 71600B Series System	
Location:	*Serial No.:*
	Tested by:
Temperature:	*Certified by:*
Humidity:	*Date:*

Performance Test Record

Page No.	Test Description		Result		
			Min	Actual	Max
	PATTERN GENERATOR				
	Clock Input Levels				
4-8	Step 9:	Waveform correct (√)			
	Step 11:	Waveform correct (√)			
	Step 12:	Clock Loss alarm present (√)			
4-9	Step 13:	Waveform correct and Clk Loss alarm present (√)			
	Clock Output Waveforms				
4-12	Step 7:	HP 70841A:			
		Rise Time - 10 to 90%			120 ps
		Fall Time - 10 to 90%			120 ps
		Preshoot			15%
		Overshoot			15%
4-13	Step 8:	HP 70841A:			
		Clock Ampl. 0.5 V:			
		Waveform correct (√)			
		Rise Time - 10 to 90%			120 ps
		Fall Time - 10 to 90%			120 ps
		Preshoot			15%
		Overshoot			15%
		Clock Ampl. 2 V:			
		Waveform correct (√)			
		Rise Time - 10 to 90%			120 ps
		Fall Time - 10 to 90%			120 ps
		Preshoot			15%
		Overshoot			15%

Performance Test Record (continued)

Page No.	Test Description	Result		
		Min	Actual	Max
4-13	Step 11: HP 70841A:			
	Clock Ampl. 2 V:			
	Waveform correct (√)			
	Rise Time - 10 to 90%			120 ps
	Fall Time - 10 to 90%			120 ps
	Preshoot			15%
	Overshoot			15%
	Clock Ampl. 1 V:			
	Waveform correct (√)			
	Rise Time - 10 to 90%			120 ps
	Fall Time - 10 to 90%			120 ps
	Preshoot			15%
	Overshoot			15%
	Clock Ampl. 0.5 V:			
	Waveform correct (√)			
	Rise Time - 10 to 90%			120 ps
	Fall Time - 10 to 90%			120 ps
	Preshoot			15%
	Overshoot			15%
	Step 15: HP 70841A:			
	Rise Time - 10 to 90%			1.3 ns
	Fall Time - 10 to 90%			1.3 ns
	Preshoot			15%
	Overshoot			15%
4-14	Step 16: HP 70841A:			
	Clock Ampl. 0.5 V:			
	Waveform correct (√)			
	Rise Time - 10 to 90%			1.3 ns
	Fall Time - 10 to 90%			1.3 ns
	Preshoot			15%
	Overshoot			15%
	Clock Ampl. 2 V:			
	Waveform correct (√)			
	Rise Time - 10 to 90%			1.3 ns
	Fall Time - 10 to 90%			1.3 ns
	Preshoot			15%
	Overshoot			15%

Performance Test Record (continued)

Page No.	Test Description		Result	
		Min	Actual	Max
	Step 19: HP 70841A:			
	Clock Ampl. 0.5 V:			
	Waveform correct (√)			
	Rise Time - 10 to 90%			1.3 ns
	Fall Time - 10 to 90%			1.3 ns
	Preshoot			15%
	Overshoot			15%
	Clock Ampl. 1 V:			
	Waveform correct (√)			
	Rise Time - 10 to 90%			1.3 ns
	Fall Time - 10 to 90%			1.3 ns
	Preshoot			15%
	Overshoot			15%
	Clock Ampl. 2 V:			
	Waveform correct (√)			
	Rise Time - 10 to 90%			1.3 ns
	Fall Time - 10 to 90%			1.3 ns
	Preshoot			15%
	Overshoot			15%
4-14	Step 22: Waveforms 180° out-of-phase (√)			
4-15	Step 31: Rising edge of pulse correct (√)			
	Data Output Waveforms			
4-19	Step 10: HP 70841A:			
	Rise Time - 10 to 90%			120 ps
	Rise Time - 20 to 80%			90 ps
	Fall Time - 10 to 90%			120 ps
	Fall Time - 20 to 80%			90 ps
	Preshoot			15%
	Overshoot			15%

Performance Test Record (continued)

Page No.	Test Description		Result		
			Min	Actual	Max
4-20	Step 12:	HP 70841A:			
		Rise Time - 10 to 90%			120 ps
		Rise Time - 20 to 80%			90 ps
		Fall Time - 10 to 90%			120 ps
		Fall Time - 20 to 80%			90 ps
		Preshoot			15%
		Overshoot			15%
	Step 15:	HP 70841A:			
		Rise Time - 10 to 90%			120 ps
		Rise Time - 20 to 80%			90 ps
		Fall Time - 10 to 90%			120 ps
		Fall Time - 20 to 80%			90 ps
		Preshoot			15%
		Overshoot			15%
4-21	Step 19:	HP 70841A:			
		Rise Time - 10 to 90%			150 ps
		Fall Time - 10 to 90%			150 ps
		Preshoot			15%
		Overshoot			15%
4-21	Step 20:	HP 70841A:			
		Clock Ampl. 0.5 V:			
		Waveform correct (√)			
		Rise Time - 10 to 90%			150 ps
		Fall Time - 10 to 90%			150 ps
		Preshoot			15%
		Overshoot			15%
		Clock Ampl. 2 V:			
		Waveform correct (√)			
		Rise Time - 10 to 90%			150 ps
		Fall Time - 10 to 90%			150 ps
		Preshoot			15%
		Overshoot			15%

Performance Test Record (continued)

Page No.	Test Description	Result		
		Min	Actual	Max
4-21	Step 23: HP 70841A:			
	Clock Ampl. 0.5 V:			
	Waveform correct (√)			
	Rise Time - 10 to 90%			150 ps
	Fall Time - 10 to 90%			150 ps
	Preshoot			15%
	Overshoot			15%
	Clock Ampl. 2 V:			
	Waveform correct (√)			
	Rise Time - 10 to 90%			150 ps
	Fall Time - 10 to 90%			150 ps
	Preshoot			15%
	Overshoot			15%
	Step 26: Waveforms 180° out-of-phase (√)			
	Trigger Output and Data Output Intrinsic Jitter			
4-24	Step 9: 32 pulses (√)			
	Step 11: Pulse Amplitude correct (√)			
	Pulse Width correct (√)			
	HP 70841A:			
4-26	Step 19:vii Intrinsic Jitter			15 ps
	PRBS 2^n-1 Pattern Length			
4-28	Step 5: 2^7-1	4095.9		4096.1
	$2^{10}-1$	32767.9		32768.1
	$2^{15}-1$	131071.9		131072.1
	$2^{23}-1$	33554431.9		33554432.1
	Step 8: 2^7-1	16255.9		16256.1
	$2^{10}-1$	130943.9		130944.1
	$2^{15}-1$	524271.9		524272.1
	$2^{23}-1$	34217711.9		34217712.1

Performance Test Record (continued)

Page No.	Test Description		Result		
			Min	Actual	Max
4-29	Step 9	2^7-1	16255.9		16256.1
		$2^{10}-1$	130943.9		130944.1
		$2^{15}-1$	524271.9		524272.1
		$2^{23}-1$	34217711.9		34217712.1
	Step 17:	2^7-1	16255.9		16256.1
	PRBS 2^n Variable Mark Density				
4-31	Step 5:	2^7 MARKDEN with mark density ratio:			
		1/8	15.9		16.1
		1/4	31.9		32.1
		1/2	31.9		32.1
		3/4	15.9		16.1
		7/8	7.9		8.1
		2^{10} MARKDEN with mark density ratio:			
		1/8	111.9		112.1
		1/4	191.9		192.1
		1/2	255.9		256.1
		3/4	191.9		192.1
		7/8	111.9		112.1
		2^{11} MARKDEN with mark density ratio:			
		1/8	223.9		224.1
		1/4	383.9		384.1
		1/2	511.9		512.1
		3/4	383.9		384.1
		7/8	223.9		224.1
		2^{13} MARKDEN with mark density ratio:			
		1/8	895.9		896.1
		1/4	1535.9		1536.1
		1/2	2047.9		2048.1
		3/4	1535.9		1536.1
		7/8	895.9		896.1

Performance Test Record (continued)

Page No.	Test Description		Result		
			Min	Actual	Max
4-32	Step 8:	2^7	127.9		128.1
		2^{10}	1023.9		1024.1
		2^{11}	2047.9		2048.1
		2^{13}	8191.9		8192.1
	Step 10:	2^7	127.9		128.1
		2^{10}	1023.9		1024.1
		2^{11}	2047.9		2048.1
		2^{13}	8191.9		8192.1
4-32	Step 17:	Ratio	127.9		128.1
4-33	Step 18:	2^{10}	1023.9		1024.1
		2^{11}	2047.9		2048.1
		2^{13}	8191.9		8192.1
	PRBS Zero Substitution				
4-35	Step 5:	2^7 ZEROSUB with longest run of zeros:			
		7 to 11	31.9		32.1
		24 to 29	27.9		28.1
		40 to 43	23.9		24.1
		55 to 59	19.9		20.1
		72 to 74	15.9		16.1
		83 to 87	11.9		12.1
		99 to 100	7.9		8.1
		114 to 115	3.9		4.1
		120 to 127	0.9		1.1
		2^{10} ZEROSUB with longest run of zeros:			
		10 to 15	255.9		256.1
		161 to 162	219.9		220.1
		320 to 322	179.9		180.1
		471 to 473	139.9		140.1
		637 to 640	99.9		100.1
		783 to 789	59.9		60.1

Performance Test Record (continued)

Page No.	Test Description		Result Min	Result Actual	Result Max
4-35	Step 5:	925 to 927	19.9		20.1
		1022 to 1023	0.9		1.1
		2^{11} ZEROSUB longest run of zeros:			
		11 to 18	511.9		512.1
		237 to 239	449.9		450.1
		636 to 643	349.9		350.1
		1065 to 1073	249.9		250.1
		1463 to 1466	149.9		150.1
		1854 to 1855	49.9		50.1
		2038 to 2039	4.9		5.1
		2046 to 2047	0.9		1.1
		2^{13} ZEROSUB longest run of zeros:			
		13 to 20	2047.9		2048.1
		1833 to 1836	1599.9		1600.1
		3365 to 3368	1199.9		1200.1
		4946 to 4949	799.9		800.1
		6616 to 6617	399.9		400.1
		7795 to 7796	99.9		100.1
		8148 to 8152	9.9		10.1
		8188 to 8191	0.9		1.1
	Error Add				
4-38	Step 11:	Reading increments by 1 (√)			
	Step 12:	Frequency 1 GHz: Reading increments by 1 (√)			
	Step 16:	Reading	31249.9		31250.1
4-39	Step 17:	Error Add Rate			
		1e −3	31.15		31.35
		1e −4	312.4		312.6
		1e −5	3124.9		3125.1
		1e −7	312499.9		312500.1
		1e −8	3124999.9		3125000.1
		1e −9	31249999.9		31250000.1

Performance Test Record (continued)

Page No.	Test Description		Result		
			Min	Actual	Max
4-39	Step 18:	Reading at 1 GHz Error Add Rate			
		1e −3	31.15		31.35
		1e −4	312.4		312.6
		1e −5	3124.9		3125.1
		1e −7	312499.9		312500.1
		1e −8	3124999.9		3125000.1
		1e −9	31249999.9		31250000.1
	User Selectable Patterns and Memory Backup				
4-42	Step 7:	Waveforms correct (√)			
4-43	Step 9:	Waveforms correct (√)			
4-44	Step 11:	Waveforms correct (√)			
	Step 13:	DC level good (√)			
4-45	Step 17:	INTERNL PATT 1	159.9		160.1
		INTERNL PATT 2	2.9		3.1
		INTERNL PATT 3	4063.9		4064.1
		INTERNL PATT 4 - DC no reading (√)			
	Step 21:	INTERNL PATT 1	159.9		160.1
		INTERNL PATT 2	2.9		3.1
		INTERNL PATT 3	4063.9		4064.1
		INTERNL PATT 4 - DC no reading (√)			
	Step 24:	INTERNL PATT 1	159.9		160.1
		INTERNL PATT 2	2.9		3.1
		INTERNL PATT 3	4063.9		4064.1
		INTERNL PATT 4 - DC no reading (√)			

Performance Test Record (continued)

Page No.	Test Description		Result		
			Min	Actual	Max
	Auxiliary Input Test				
4-50	Step 7:	Pulse able to inhibit PRBS at *DATA OUT* port (√)			
	Step 8:	Pulse able to inhibit PRBS at *DATA OUT* port at each of the following frequencies: 499 MHz (√) 500 MHz (√) 1 GHz (√) 3 GHz (√)			
4-52	Step 14:	Correct reading (√)	0.9		1.1
	Step 15:	Correct reading at the following frequencies:			
		499 MHz (√)	0.9		1.1
		500 MHz (√)	0.9		1.1
		1 GHz (√)	0.9		1.1
		3 GHz (√)	0.9		1.1

Performance Test Record (continued)

Page No.	Test Description	Result Min	Result Actual	Result Max
	ERROR DETECTOR			
	Clock Input Levels			
4-59	Step 7: No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
	Step 8: No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
	Step 10: Clk Loss alarm present (√)			
	Step 13: No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
	PRBS 2^n-1 Pattern Synchronization, Error Detect and Audible Beep			
4-61	Step 4: No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
	Step 6: No Clk Loss, Data Loss, Sync Loss or Errors alarms present at each of the following PRBS: $2^{31}-1$(√) $2^{15}-1$(√) $2^{10}-1$(√) $2^{7}-1$(√)			
4-62	Step 12: Audible beep heard (√)			
	Step 13: Error count is 1 (√)			

Performance Test Record (continued)

Page No.	Test Description	Result		
		Min	Actual	Max
4-62	Step 14: Audible beep sounds and the error count increments by 1 each time the key is pressed (√)			
	Step 16: Audible beep sounds and error count increments with each of the following PRBS settings: $2^{10}-1$ (√) $2^{15}-1$ (√) $2^{23}-1$ (√) $2^{23}-1$(√)			
	Step 17: Maximum module frequency: Audible beep sounds and error count increments at each of the following PRBS: $2^{7}-1$ (√) $2^{10}-1$ (√) $2^{15}-1$ (√) $2^{23}-1$ (√) $2^{23}-1$ (√)			
	Step 21: Errors alarm present (√)			
4-63	Step 24: Typical error ratio correct (√)			
	Step 25: Typical error ratio and delta error ratio correct with the following PRBS: $2^{23}-1$(√) $2^{15}-1$ (√) $2^{10}-1$ (√) $2^{7}-1$ (√)			

Page No.	Test Description	Result		
		Min	Actual	Max
4-63	Step 27: Error ratio and delta error ratio correct at 3 GHz with the following PRBS:			
	Step 27: $2^{23}-1$ (√) $2^{23}-1$ (√) $2^{15}-1$ (√) $2^{10}-1$ (√) $2^{7}-1$ (√)			
	PRBS 2^n Pattern Synchronization, Error Detect and Memory Backup			
4-65	Step 5: No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
4-66	Step 7: No Clk Loss, Data Loss, Sync Loss or Errors alarms present at each of the following PRBS: 2^{10} MARKDEN (√) 2^{11} MARKDEN (√) 2^{13} MARKDEN (√)			
	Step 12: Error count is 1 (√)			
	Step 13: Error count increments by 1 and audible beep sounds each time the key is pressed (√)			
	Step 15: Error count increments by 1 and audible beep sounds each time the key is pressed at the following PRBS: 2^{11} MARKDEN (√) 2^{10} MARKDEN (√) 2^{7} MARKDEN (√)			

Performance Test Record (continued)

Page No.	Test Description		Result		
			Min	Actual	Max
4-66	Step 16:	Maximum module frequency: Error count increments by 1 and audible beep sounds each time the key is pressed at the following PRBS: 2^7 MARKDEN (√) 2^{10} MARKDEN (√) 2^{11} MARKDEN (√) 2^{13} MARKDEN (√)			
	Step 20:	Errors alarm present (√)			
4-67	Step 23:	Typical error ratio correct (√) Typical delta error ratio correct (√)			
	Step 24:	Typical Error ratio and delta error ratio correct at the following PRBS: 2^{10} MARKDEN (√) 2^{11} MARKDEN (√) 2^{13} MARKDEN (√)			
	Step 26:	Typical Error ratio and delta error ratio correct at the following PRBS: 2^7 MARKDEN (√) 2^{10} MARKDEN (√) 2^{11} MARKDEN (√) 2^{13} MARKDEN (√)			
	Step 29:	Time/date correct (√)			
	Step 30:	Power Loss Second displayed(√)			

Performance Test Record (continued)

Page No.	Test Description	Result		
		Min	Actual	Max
	PRBS 2^n Pattern with Variable Mark Density			
4-69	Step 5: No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
	Step 8: Sync Loss and Errors alarms present (√)			
	Step 11: No Sync Loss or Errors alarms (√)			
4-70	Step 16: Error count increments by 1 (√)			
	Step 17: Error count increments by 1 and Erorrs Alarm flashes each time the key is pressed (√)			
	Step 19: Error count increments and the Errors Alarm flashes each time the key is pressed at the following mark densities: 1/4 (√) 3/4 (√) 7/8 (√)			
	Step 20: Error count increments and the Errors Alarm flashes each time the key is pressed when the			
	Step 20: PRBS and mark densities are as following:			

Performance Test Record (continued)

Page No.	Test Description	Result		
		Min	Actual	Max
4-70	2^{10} MARKDEN: 1/8 (√) 1/4 (√) 3/4 (√) 7/8 (√) 2^{11} MARKDEN: 1/8 (√) 1/4 (√) 3/4 (√) 7/8 (√) 2^{13} MARKDEN: 1/8 (√) 1/4 (√) 3/4 (√) 7/8 (√) Step 22: Maximum module frequency: Error count increments and the Errors alarm flashes each time the key is pressed when the PRBS and mark densities are as following: 2^{10} MARKDEN: 1/8 (√) 1/4 (√) 3/4 (√) 7/8 (√) 2^{11} MARKDEN: 1/8 (√) 1/4 (√) 3/4 (√) 7/8 (√) Step 22: 2^{13} MARKDEN: 1/8 (√) 1/4 (√) 3/4 (√) 7/8 (√)			

Performance Test Record (continued)

Page No.	Test Description		Result		
			Min	Actual	Max
	PRBS 2^n Pattern with Zero Substitution				
4-72	Step 5:	No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
4-73	Step 8:	No Clk Loss, Data Loss, Sync Loss or Errors alarms present and that the resync times are as follows:			
		Resync time for 2^7 ZEROSUB with the following longest run of zeros; 7, 20, 40, 80, 84, 89 and 90			2 s
		Resync time 2^{10} ZEROSUB with the following longest run of zeros; 10, 200, 400, 600, 750, 794 and 795			2 s
		Resync time for 2^{11} ZEROSUB with the following longest run of zeros; 11, 400, 800, 1200, 1550, 1599 and 1600			2 s
	Step 8:	Resync time 2^{13} ZEROSUB with the following longest run of zeros; 13, 2400, 5600, 6398 and 6400			2 s
	Step 9:	No Clk Loss, Data Loss, Sync Loss or Errors alarms present and that the resync times at the maximum module frequency is as follows:			

Performance Test Record (continued)

Page No.	Test Description	Result		
		Min	Actual	Max
4-73	Resync time for 2^7 ZEROSUB with the following longest run of zeros; 7, 20, 40, 80, 84, 89 and 90			2 s
	Resync time 2^{10} ZEROSUB with the following longest run of zeros; 10, 200, 400, 600, 750, 794 and 795			2 s
	Resync time for 2^{11} ZEROSUB with the following longest run of zeros; 11, 400, 800, 1200, 1550, 1599 and 1600			2 s
	Step 9: Resync time 2^{13} ZEROSUB with the following longest run of zeros; 13, 2400, 5600, 6398 and 6400			2 s
	User Selectable Pattern Synchronization and Error Detect			
4-76	Step 6: No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
	Step 7: No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
	Step 12: Error count is 1 (√)			
	Step 13: Error count increments by 1 and Errors Alarm flashes each time the key is pressed (√)			

Page No.	Test Description	Result		
		Min	Actual	Max
4-76	Step 15: Error count increments by 1 and Errors Alarms flashes each time the key is pressed with the frequency set to the maximum module frequency (√) Step 17: Error count increments by 1 and Errors Alarms flashes each time the key is pressed with the frequency and PRBS set as follows: Minimum module frequency: INTERNL PATT 2 (√) INTERNL PATT 3 (√) INTERNL PATT 4 (√) Maximum module frequency: INTERNL PATT 2 (√) INTERNL PATT 3 (√) INTERNL PATT 4 (√)			

Performance Test Record (continued)

Page No.	Test Description	Result Min	Result Actual	Result Max
	Data Input Range (Automatic 0/1 Threshold)			
4-79	Step 11: No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
	Step 12: No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
	Step 13: No Clk Loss, Data Loss, Sync Loss or Errors alarms present			
4-80	Step 16: No Clk Loss, Data Loss, Sync Loss or Errors alarms present with DATA AMPLITUDE and DATA HI LEVEL set as follows:			
	Step 16:			
	Data Ampl — Data Hi			
	500 mV — 1 V (√)			
	500 mV — −2.5 V(√)			
	2 V — 1 V (√)			
	2 V — −1 V (√)			
	Step 21: No Clk Loss, Data Loss, Sync Loss or Errors alarms present with DATA AMPLITUDE and DATA HI LEVEL set as follows:			
	Data Ampl — Data Hi			
	500 mV — 0V (√)			
	500 mV — −2.5 V (√)			
	2 V — 0 V (√)			
	2 V — −1 V (√)			

Performance Test Record (continued)

Page No.	Test Description		Result	
		Min	Actual	Max
	Error Output Waveform and Data Input Delay			
4-82	Step 4: No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
4-83	Step 10: No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
	Step 12: Errors alarm indicated and displayed (√)			
	Step 15: Typical Error ratio correct (√)			
4-84	Step 18: Typical Pulse Amplitude correct (√) Typical Pulse Width correct (√)			
	Step 22: Sync lost and regained as delay is reduced (√)			
	Data Input Invert			
4-86	Step 5: No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
	Step 11: No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
	Step 15: No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
	Step 17: Sync Loss and Errors alarms present (√)			

Performance Test Record (continued)

Page No.	Test Description	Result Min	Result Actual	Result Max
4-87	Step 20: No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
	Step 22: Sync Loss and Errors alarms present (√)			
	Step 26: No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
	Pattern Synchronization Threshold			
4-89	Step 5: No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
	Step 10: No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
4-90	Step 13: Sync Loss and Errors alarms present (√)			
	Step 15: No Sync Loss alarm present (√)			
	Step 19: Typical Error ratio correct (√)			
	Step 26: No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
4-91	Step 28: Sync Loss and Errors alarms present (√)			
	Step 30: No Sync Loss alarm (√)			

Performance Test Record (continued)

Page No.	Test Description		Result	
		Min	Actual	Max
4-91	Step 32: Typical Error ratio correct (√)			
	Step 35: Sync Loss and Errors alarms present (√)			
	Step 37: Sync Loss and Errors alarms present (√)			
	Step 39: No Sync Loss and Errors alarms present (√)			
4-92	Step 47: No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
	Resync time			2.0 secs
	Step 49: Sync Loss and Errors alarms present (√)			
	Step 51: No Sync Loss alarm present (√)			
	Step 53: Typical Error ratio correct (√)			
	Step 59: No Clk Loss, Data Loss, Sync Loss or Errors alarms present (√)			
	Resync time			2.0 secs
	Step 61: Sync Loss and Errors alarms present (√)			

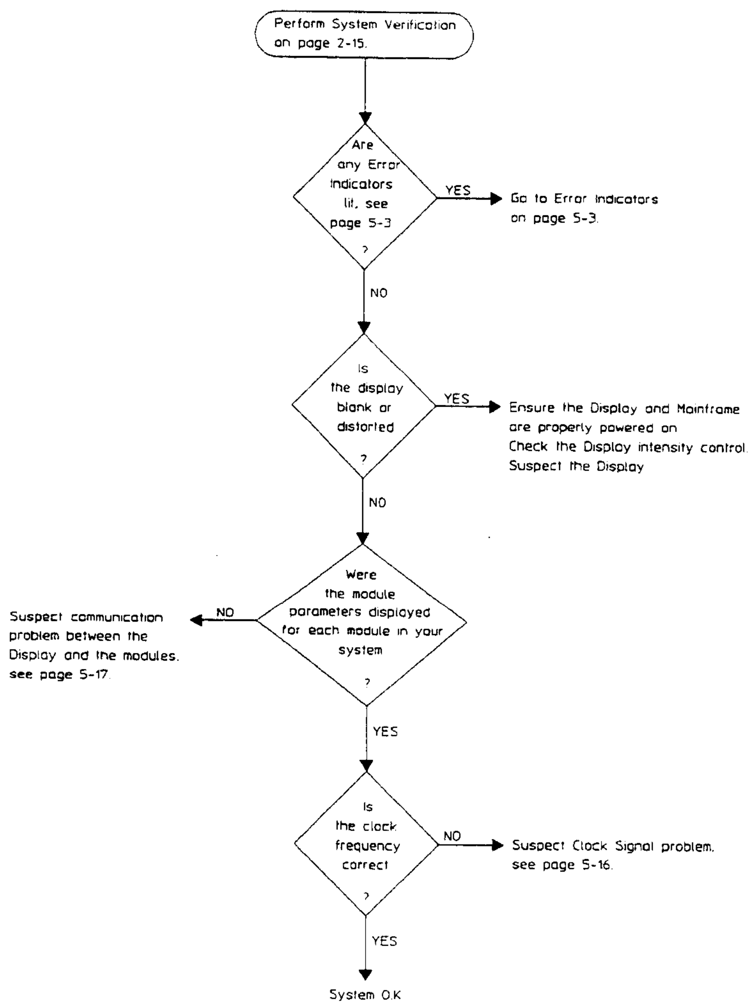
5

Troubleshooting

The aim of this chapter is to help you identify the fault in your system.

Entry Chart

All troubleshooting starts from the Entry Chart below:



System Indicators

Each element in the system has indicators to help with problem identification. The following indicators are fitted:

Error Indicators These tell the user that there is a failure within the system.

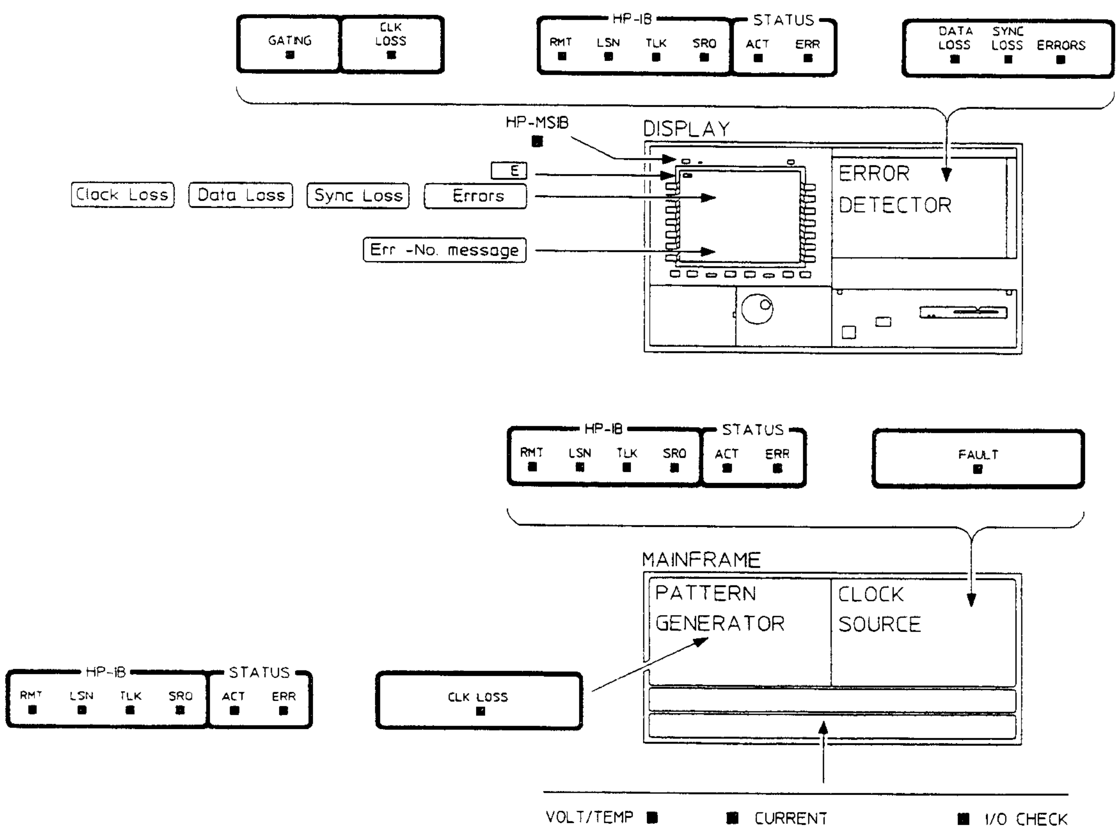
Error Messages These appear on the display and perform the same function as the *Error Indicators*.

Active (ACT) Indicators These tell the user which element is currently active in the system.

HP-IB Indicators These tell the user the current HP-IB status of each element.

Gating Indicator This is fitted to the *Error Detector* module and indicates when a BER measurement is is progress.

The following diagram will help you locate the indicators in your system:



Error Indicators

The error indicators and associated troubleshooting information is contained in the following table. Troubleshoot the error indicators in the order given.

Error Indicator	Location	Meaning	Page
VOLT/TEMP	Mainframe	A low input ac voltage detected or an ambient temperature > 55 °C.	5-4
CURRENT	Mainframe	A high current load on Mainframe power supplies.	5-5
E (flashing)	Display (CRT)	An HP-MSIB problem has been detected at power on. This may affect normal communication between modules (may affect *Error Reporting*).	5-6
ERR (flashing)	Any module		
HP-MSIB	Display (front panel)	An HP-MSIB problem has been detected.	
I/O CHECK	Mainframe		
FAULT	Clock Source	Module faulty - refer to *Clock Source* Service manual.	
E (steady)	Display (CRT)	A master module or the display has detected an error.	5-8
ERR (steady)	Module or Clock Source	The element has an error condition. If the element is a slave, then the *error indicator* of the slave and its master will be lit.	
CLK LOSS	Pattern Generator or Error Detector	The module has not detected the incoming clock signal.	5-16
DATA LOSS	Error Detector	The module has not detected the incoming data over a 1 ms gating period.	5-16
SYNC LOSS	Error Detector	The module has been unable to synchronize to the incoming data pattern.	5-17
ERRORS	Error Detector	The module has detected *Bit Errors* in the incoming data pattern.	5-17

VOLT/TEMP Troubleshooting

The *VOLT/TEMP* indicator on the Mainframe is lit when one of the following conditions occur:

A low line voltage is applied to the Mainframe.

The ambient temperature inside the Mainframe is > 55 °C.

Use the following procedure to determine the cause of the fault:

1. Power down the system and disconnect the mains power cable from the Mainframe, then check that the Mainframe *VOLTAGE SELECTOR* switch is set correctly:

   115 V position for 90 - 132 Vac line input voltage.
   230 V position for 198 - 264 Vac line input voltage.

2. Check that the line input voltage is within specification.

Note If the voltage increases to within the normal operating range, the Mainframe will restart itself.

If the *VOLTAGE SELECTOR* switch and input line voltage are correct, suspect excessive ambient temperature inside the Mainframe.

3. Check that the fan is operating correctly by checking the air flow at the fan-intake openings.

Note It is recommended that the fan filters be regularly cleaned, as a build up of dust on the filters will reduce the airflow into the Mainframe.

If the temperature decreases to within the normal operating range, the Mainframe will restart itself.

If all the above are good then the Mainframe is faulty, go to the *Mainframe Service Manual* for troubleshooting information.

CURRENT Troubleshooting

The *CURRENT* indicator on the Mainframe is lit when excessive current is detected.

Note The Mainframe will not attempt to restart until the power has been cycled.

Use the following procedure to determine the cause of the fault:

1. Power down your system.
2. Remove any module(s) from the Mainframe.
3. Power on the system.
4. Is the *CURRENT* indicator still lit?

   If YES, then the Mainframe is faulty, go to the Mainframe Service Manual *for troubleshooting information.*
   If NO, then suspect the module(s).

HP-MSIB Troubleshooting

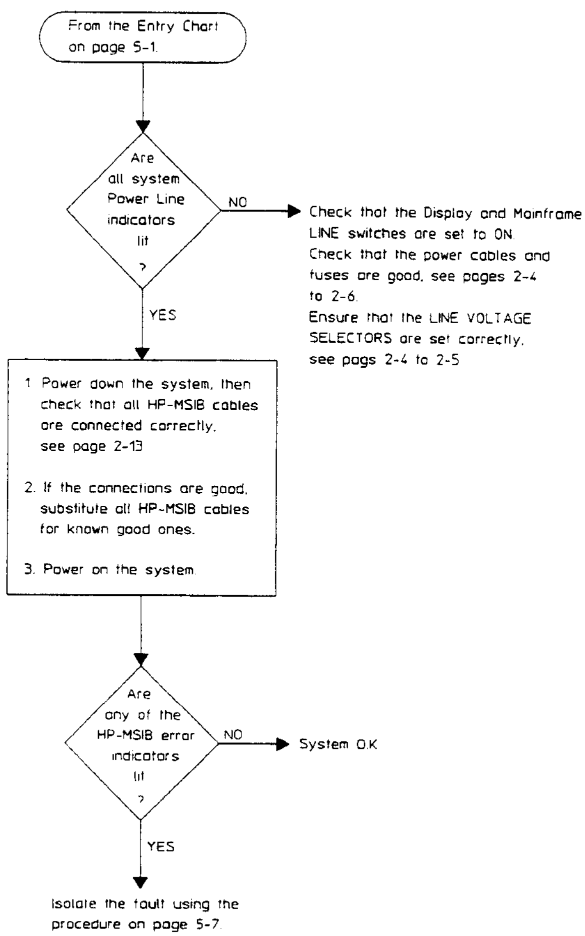
An HP-MSIB failure exists if any of the following indicators are lit:

E (flashing) on the display.
ERR (flashing) on a module.
HP-MSIB lit on the Display front panel.
I/O CHECK lit on the Mainframe front panel.

The flashing *E* and *ERR* only occur at power on. When these occur normal communication between the Display and other elements in the system may be prevented. The cause of this failure must be found before any predictable system operation can take place.

The possible causes of an HP-MSIB failure are as follows:

Display, Mainframe or Clock Source not powered on
Poor HP-MSIB cable connection or faulty cable
Faulty Display
Faulty Mainframe
Faulty Module(s)



Use the following procedure to troubleshoot all HP-MSIB error indicators:

1. Isolate all elements in your system as follows:
   i. Power down your system.
   ii. Disconnect all HP-MSIB cables.
   iii. Remove module(s) from the Display and Mainframe (if your system has one).
2. Check the Display as follows:
   i. Power on the Display.
   ii. Is there an *E* (flashing or steady) on the display?

      If YES, then the Display is faulty.
      If NO, power down the Display then go to step iii.
   iii. Connect a known good HP-MSIB cable between the *IN* and *OUT HP-MSIB* ports on the rear panel of the Display, then power on.
   iv. Is there an *E* (flashing or steady) on the display?

      If YES, then the Display is faulty.
      If NO, power down the Display, remove the HP-MSIB *cable, then go to step 3*
3. Check the module(s) as follows:
   i. Plug a module into the Display, then power-on.
   ii. Is there an *E* flashing on the Display or *ERR* flashing on the module?

      If YES, then the module is faulty.
      If NO, power down the Display then repeat step 3 for each module in your system.
      If all modules are good, power down the Display then go to step 4.
4. Check the Mainframe as follows:
   i. Connect known good HP-MSIB cables between the *IN* and *OUT HP-MSIB* ports on the rear panel of the Display and Mainframe (see page 2-13), then power on.
   ii. Is there an *E* (flashing or steady) on the display, or is the *HP-MSIB* or *I/O CHECK* indicator lit?

      If any error indicator is lit, check that the Display and Mainframe are properly powered on and that the HP-MSIB cabling is correct. If these are good, and E is still flashing on the display then the Mainframe is faulty.

MMS Error Messages

MMS error messages are available when a steady *E* is displayed or a steady *ERR* indicator is lit (if the module is a slave, its masters *ERR* indicator is also lit). MMS error messages break down into two groups, a general summary of each is given below:

Instrument Specific Errors	These error messages are specific to the HP 71600 Series and are positive numbers. They are divided into *permanent* and *non-permanent* fault conditions, see pages 5-9 to 5-15.
Standard Commands for Programming Instruments (SCPI)	These error messages apply to any Modular Measurement System and are negative numbers. They are divided into three groups; Command Errors, Execute Errors and Query Errors.

Error messages appear automatically at the bottom of the display or are accessed through the *Error Reporting* function on the display.

Error Reporting

When an *E* appears on the display or an *ERR* indicator is lit and an error message is not automatically displayed the following procedure enables you to access the *Error Reporting* function on the display:

1. Press the (DISPLAY) key.
2. Press the REPORT ERRORS softkey. If more than one element has reported errors, use the MORE ERRORS softkey, see the following page for *Error Messages*.

When errors are reported by a master, the model number and HP-MSIB address of the element that generated the error are displayed.

Note After the errors have been read they are cleared from the system memory (except for permanent errors).

The tables on the following pages contain *Non-permanent Errors, Permanent Errors* and *SCPI Errors.*

Non-permanent Errors

Error No.	Displayed Message	Description	Applicability*
101	Invalid set option		edet + pgen
102	Invalid query option		edet + pgen
103	Already gating	The instrument cannot be commanded to start gating while it is already gating.	edet
104	Already not gating	The instrument cannot be commanded to end gating while it is already not gating.	edet
105	Not while gating	This command is not permitted while the instrument is gating.	edet
106	Cannot gate while centering	This command is not permitted while the instrument is centering the eye height.	edet
107	Cannot gate while aligning	This command is not permitted while the instrument is aligning the eye width.	edet
108	Clock attenuator too large.		pgen
109	Keyboard locked	Commands that change the instrument's configuration are not permitted while the keyboard is locked.	edet + pgen
110	Window too small:		edet + pgen
111	Conflicts with run of zeros	The zero-substitution pattern requested is incompatible with the current setting of the run of zeros.	edet + pgen
112	Conflicts with zsub length	The run of zeros requested is incompatible with the current setting of the zero-substitution length.	edet + pgen
113	Conflicts with data high level	The data amplitude requested is incompatible with the current setting of the data high level.	pgen
114	Conflicts with data amplitude	The data high level requested is incompatible with the current setting of the data amplitude.	pgen
115	Need 2 adjacent locations	This item cannot be added to the User's Page because it needs two adjacent locations.	edet
116	Logging already enabled	The instrument cannot be commanded to start logging while logging is already enabled.	edet

Non-permanent Errors (continued)

Error No.	Displayed Message	Description	Applicability*
117	Logging already disabled	The instrument cannot be commanded to end logging while logging is already disabled.	edet
118	Not while logging enabled	This command is not permitted while the instrument has logging enabled.	edet
119	Slave needs service	The slave module has detected an error and is requesting that its error queue be read to identify the cause.	edet + pgen
120	Data attenuator too large	The instrument cannot produce the defined ECL levels with the current value of attenuator.	pgen
121	Slave not present	The command can be executed only if a slave module exists.	edet + pgen
122	Need 4 adjacent locations	This item cannot be added to the User's Page because it needs four adjacent locations.	edet
123	Do not have system clock	The date or time cannot be set in this instrument as it is not the holder of the system date and time (ie there is another module from which it picked up the date and time at power up).	edet
124	Cannot align data if gating	A Clock to Data Align cannot be performed while we are gating as it interferes with the calculation of measurement results.	edet
125	Cannot center if gating	A 0/1 Threshold Center cannot be performed while we are gating as it interferes with the calculation of measurement results.	edet
126	Cannot align data if centering	A Clock to Data Align cannot be performed while we are performing a 0/1 threshold center operation.	edet
127	Cannot center data if aligning	A 0/1 threshold center operation cannot be performed while we are performing a Clock to Data Align operation.	edet
128	Already have external controller	The CONTROLLER capability cannot be used when an external HP-IB controller is already connected.	edet

Non-permanent Errors (continued)

Error No.	Displayed Message	Description	Applicability*
129	Address conflicts with Err Det	Cannot set the printer address to that of the Error Detector.	edet
174	Non-volatile memory error	The non-volatile memory has failed causing the previous instrument setup to be lost.	edet + pgen
175	Results corrupted	The non-volatile memory has failed causing the measurement results to be lost.	edet
400	Pattern too large for store:		edet + pgen
401	Cursor position outside range:		edet + pgen
402	Invalid pattern length	The chosen length for the pattern cannot be generated by the instrument. The length must lie within the specified resolution. Only generated when the user pattern memory is active.	pgen + edet
403	Pattern length out of range	The pattern length is too large for the store.	pgen + edet
404	Invalid char(s) in label	A character in the label is not valid.	pgen + edet
405	Alternate patterns have no trigger bit	Alternate patterns do not have a trigger bit position. It is an error to try and set the trigger bit for a pattern store containing an alternate pattern.	pgen + edet
406	Straight patterns have no trigger mode	Straight patterns do not have a trigger mode. It is an error to try and set the trigger mode for a pattern store containing a straight pattern.	pgen + edet
407	Pattern store label too long	The label for the pattern store exceeds the maximum length allowed.	pgen + edet
408	Invalid pattern store	The pattern store number does not identify a valid store.	pgen + edet
409	Straight patterns have no half B	Attempt to perform an operation specific to an alternate pattern when the pattern store contains a straight pattern.	pgen + edet
410	Disk drive disabled	The disk drive has been internally disabled. The requested action on the disk drive can not be performed.	pgen

Non-permanent Errors (continued)

Error No.	Displayed Message	Description	Applicability*
411	Disk pattern header invalid	An error has been detected in the information within the file holding the pattern store data. The file may be corrupted.	pgen
414	Disk pattern store invalid	The index field in the file containing the pattern store data is set to an illegal value. The file may be corrupted.	pgen
415	Disk pattern type invalid	The pattern type field in the file containing the pattern store data is set to an illegal value. The file may be corrupted.	pgen
416	Disk pattern label invalid	The pattern label in the file containing the pattern store data contains an illegal character. The file may be corrupted.	pgen
417	Internal disk error	Internal failure in disc system	pgen
418	Unrecognised disk error	An unrecognized error has occured whilst using the disk.	pgen
419	Directory overflow	Directory Overflow. Although there may be room on the media for the file, there is no room in the directory for another file name.	pgen
420	Pattern file not found	There is no file corresponding to the pattern store on the disc.	pgen
421	End of pattern file error	Operation caused the end of file to be reached. No data left whilst reading, or space left when writing to a pattern store.	pgen
422	Disk full	The disk is full. There is not enough free space for the specified size of pattern store.	pgen
423	Bad disk controller	There is a hardware problem with the floppy disk control electronics.	pgen
424	File open on disk	Operation not allowed on open file. May arise after changing the disk whilst an operation is in progress.	pgen
425	Media changed or not in drive	Disk changed or not in drive. Either there is no disc in the drive, or the eject button is pressed whilst the disk is being accessed.	pgen

Non-permanent Errors (continued)

Error No.	Displayed Message	Description	Applicability*
426	Bad disk drive	Mass storage unit not present. A hardware problem.	pgen
427	Disc write protected	Write protected. Attempting to change the contents of a disk with it's write-protect tab set. Saving to a pattern store on disk, deleting a pattern store from the disk, or formatting a disk all generate this error if the disk is write-protected.	pgen
428	Disk media uninitialized	Media not initialized. The disk must be formatted before it is used to store pattern information.	pgen
429	Disk data read error	Read data error. The media is physically or magnetically damaged, and the data can not be read.	pgen
430	Disk check read error	Checkread error. An error was detected when reading the data just written. The media is probably damaged.	pgen
431	Corrupt disk	Disc may be corrupt.	pgen
435	Unable to reload edit buffer	During power-on, the user pattern memory could not be reloaded from the appropriate pattern store.	pgen

Permanent Errors

Error No.	Displayed Message	Description	Applicability*
	Error codes associated with interface 1 board		
130	Interface 1 board missing	The Interface 1 board is not present in the instrument.	edet + pgen
134	Too much calibration data	There is too much Phase Shifter (Vernier) calibration data to be held internally by the firmware. This must mean a bad calibration or that the calibration method has changed and this firmware is out of date.	edet + pgen
135	Vernier not calibrated	The calibration data for the Phase Shifter Vernier has been corrupted in the EEPROM.	edet + pgen
136	EEPROM sync-loss contents error	The calibration data for sync-loss detection has been corrupted in the EEPROM.	edet
137	EEPROM module ID error.	The calibration data for module identification has been corrupted in the EEPROM.	edet
	Error codes associated with interface 2 board		
140	Interface 2 board missing	The Interface 2 board is not present in the intrument.	pgen
143	Interface 2 freq meas error	The self-test firmware detected that a frequency measurement could not be started correctly.	pgen
144	EEPROM data contents error	The calibration data for the data amplifier has been corrupted in the EEPROM.	pgen
145	EEPROM clock contents error	The calibration data for the clock amplifier has been corrupted in the EEPROM.	pgen
146	EEPROM crc error:		edet + pgen
	Error codes associated with gate array board		
150	Gate array board missing	The Gate Array board is not present in the instrument.	edet + pgen
153 to 168	Gate array RAM (U3 - U18) error:	The self-test firmware detected a problem with writing to and reading from the ECL RAM CHIP U3 - U18 on the Gate Array board.	edet + pgen

Permanent Errors (continued)

Error No.	Displayed Message	Description	Applicability*
170 to 173	Ram (U8 - U11) error:	The Self-test firmware detected a problem with writing reading from the RAM on the Control Processor Board U8 - U11.	pgen + edet
174		See the section on Non-Permanent errors	
175		See the section on Non-Permanent errors	
176		NV-RAM (U22) error:	
177		NV-RAM (U23) error:	
	Error codes associated with ROM		
180	ROM (U6) error	The self-test firmware detected an error during the CRC check of the Read Only Memory (ROM) on the Control Processor Board U6.	edet + pgen
181	ROM (U7) error	The self-test firmware detected an error during the CRC check of the Read Only Memory (ROM) on the Control Processor Board U7.	edet + pgen
185	PIT contents corrupt:	The Peripheral Interface/Timer (PI/T) device on the Control Processor board is not correctly retaining the values placed in it's Timer Preload Registers.	pgen + edet
186	PIT timer failure:	The Peripheral Interface/Timer (PI/T) device on the Control Processor board is not correctly counting time.	pgen + edet
	Error codes associated with HP-MSIB		
190	MSIB error	The internal self-test of the HP-MSIB bus has detected an error.	edet + pgen
191	Unrecognised slave found	An unrecognised MMS module has been found in this module's slave address space.	edet + pgen
192	Too many slaves found	More than the permitted number of slaves have been found in this module's slave address space.	edet + pgen

Permanent Errors (continued)

Error No.	Displayed Message	Description	Applicability*
193	Slaved patt gen f/w incompatible	The firmware version of the slaved Pattern Generator is too old to be compatible.	edet
194	Slaved clock f/w incompatible	The firmware version of the slaved clock is too old to be compatible.	pgen
	Error codes associated with measurement processor		
200	Measurement board missing	The Measurement Processor board is not present in the instrument.	edet
201	DPRAM test error	The Self-test firmware detected a problem with writing to and reading from the Dual Port RAM (DPRAM) on the Control Processor Board U28.	edet
202	DPRAM exchange error	An error occurred in the firmware when we tried to create an exchange for processing results.	edet
203	DPRAM initialisation error	An error occurred in the firmware when trying to set up the firmware for processing of results from the DPRAM.	edet
204	DPRAM timeout error	The Control Processor firmware timed out while waiting for a response to a command sent to the Measurement Processor.	edet
205	Invalid DPRAM command	An invalid command has been sent via DPRAM to the Measurement Processor from the Control Processor.	edet
207	Results missed error	One or more sets of results from the Measurement Processor has been missed by the Control Processor.	edet
208	Measurement firmware incompatible	The firmware in the Measurement Processor is incompatible with the firmware in the control processor.	edet
210	Pattern type protocol error	An invalid pattern type command has been sent to the Measurement processor from the control processor.	edet
211	Pattern length protocol error #1	An invalid pattern length command has been sent to the Measurement processor from the control processor.	edet

Permanent Errors (continued)

Error No.	Displayed Message	Description	Applicability*
212	Polarity protocol error	An invalid pattern polarity command has been sent to the Measurement processor from the control processor.	edet
213	Sync protocol error	An invalid sync command has been sent to the Measurement processor from the control processor.	edet
214	Threshold protocol error	An invalid sync threshold command has been sent to the Measurement processor from the control processor.	edet
215	Clock edge protocol error	An invalid clock edge command has been sent to the Measurement processor from the control processor.	edet
216	Pattern length protocol error #2	An invalid pattern length command has been sent to the Measurement processor from the control processor.	edet
217	Header protocol error	An invalid command has been sent to the Measurement processor from the control processor.	edet
218	Measurement board ROM (U3) error	The self-test firmware detected an error during the CRC check of the Read Only Memory (ROM) on the Measurement Processor Board U3.	edet
219	Measurement board ROM (U4) error	The self-test firmware detected an error during the CRC check of the Read Only Memory (ROM) on the Measurement Processor Board U4.	edet
220	Measurement board RAM (U5) error	The Self-test firmware detected a problem with writing to and reading from the RAM on the Measurement Processor Board U5.	edet
221	Measurement board RAM (U6) error	The Self-test firmware detected a problem with writing to and reading from the RAM on the Measurement Processor Board U6.	edet

Permanent Errors (continued)

Error No.	Displayed Message	Description	Applicability*
222	Measurement board PIT timer error	The Peripheral Interface / Timer (PI/T) device on the Measurement Processor board is not correctly counting time.	edet
223	Measurement board PIT contents error	The Peripheral Interface / Timer (PI/T) device on the Measurement Processor board is not correctly retaining the values placed in it's Timer Preload Registers.	edet
224	Pattern length protocol error #3	An invalid pattern length command has been sent to the Measurement processor from the control processor.	edet

*edet=Error Detector; pgen=Pattern Generator

Standard Commands for Programming Instruments (SCPI)

Command Error (CME)	Execute Error (EXE)	Query Errors (QYE)
-100 to -199	-200 to -299	-400 to -499
For more details on programming errors, see the *HP 71600 Series System Programming Manual.*		

Clock Loss Troubleshooting

If the clock frequency shown on the display is incorrect or if the *CLK LOSS* indicator is lit on either the *Error Detector* or *Pattern Generator* module, suspect that one of the following is faulty:

Clock Source module.
Cable connecting Clock Source module *CLOCK OUT* port to *CLOCK IN* port on module(s)
Module(s)

Note The *CLK LOSS* indicator will be lit if clock signal is typically < -10 dBm.

If your system is an *Error Performance Analyzer* and the *CLK LOSS* indicator is lit on both the *Error Detector* and *Pattern Generator* modules, suspect the Clock Source or one of the cables. If only one indicator is lit, then suspect the cables or the module.

If the Error Detector module is suspect, connect the Clock Source *CLOCK OUT* port to the Error Detector *CLOCK IN* port. If the *CLK LOSS* indicator is still lit the Error Detector is faulty.

If your systerm is a *Pattern Generator* - suspect the cables or modules.

To troubleshoot both systems first check the output of the Clock Source then use known good cables - if still faulty then suspect the module.

Clock Source Output

Access the Clock Source setup on the Display (see *Operating Manual*), check that the Clock Source Output is set to *ON*. Check that the frequency of the Clock source has been set within the range of the system, 100 MHz to 3 GHz for the HP 71603B/HP 71604B. If correct, use an Oscilloscope or Power Meter to check the output level is > -10 dBm. If good, the Clock Source is good.

DATA LOSS Troubleshooting

The *DATA LOSS* indicator is lit on *Error Detector* when no data transitions have been detected over a 1 ms period. Normally, if there is a loss of input signal the *SYNCH* and *ERRORS* indicators will be lit. A loss of clock signal may also cause the *DATA LOSS* indicator to light, see *CLK LOSS Troubleshooing*.

To troubleshoot the systems first check the data being applied to the *Error Detector* and use known good cables - if still faulty then suspect the module.

Note The Error Detector *DATA IN* port is very sensitive and will trigger on background noise.

SYNC LOSS and ERRORS Troubleshooting

If either of these indicators is lit, check that the Error Performance Analyzer verification procedure has been performed correctly. If good, suspect Clock or Data cabling between modules or a fault in the Pattern Generator or Error Detector module.

Communication Troubleshooting

If you are unable to access the module(s) in your system through the Display - no communication between the Display and the module(s) - and there are no error indicators lit, use the following procedure to isolate the fault:

1. Check all modules have been set to valid HP-MSIB addresses, see pages 6-5 to 6-8.
2. Isolate all elements in your system as follows:
   - i. Power down your system.
   - ii. Disconnect all HP-MSIB cables.
   - iii. Remove module(s) from the Display and Mainframe (if your system has one).
3. Check that the Display can access all 31 addresses on *row 0* as follows:
   - i. Power on the Display.
   - ii. Press (DISPLAY) and `Address Map`.
   - iii. Use the front panel control knob to scroll the green rectangle (on the display) along the 31 addresses on *row 0*.

     If a red rectangle appears, the Display is faulty.

     If you can access the addresses, the Display is good. Power down the Display then go to step 3.
4. Check the module(s) as follows:
   - i. Plug a module into the Display.
   - ii. Power on the Display.
   - iii. Check that the Display can access all 31 addresses on *row 0*, use the procedure in step 2.

     If a red rectangle appears, the module is faulty.

     If you can access the addresses, the module is good, power down the Display then repeat step 3 for each module in your system.

     If all modules are good, power down the Display, remove the module then go to step 4.

5. Check the Mainframe as follows:

   i. Connect known good HP-MSIB cables between the *HP-MSIB IN* and *OUT* ports on the rear panel of the Display and Mainframe (see page 2-13).

   ii. Power on the Display and Mainframe.

   iii. Check the Display can access all 31 addresses on *row 0*, use the procedure in step 2.

      If a red rectangle appears, the Mainframe is faulty.

      If you can access the addresses, the Mainframe is good.

6

HP 71600 Series (a Modular Measurement System)

Your HP 71600 Series (*Error Performance Analyzer* and *Pattern Generator*) is made up of a Display, Mainframe and Module(s). These are linked together by a bus system called the Hewlett-Packard Measurement System Interface Bus (HP-MSIB) to form a Modular Measurement System (MMS). The HP 71600 Series can be configured as a master/slave MMS or a master/master MMS. The information is presented under the following headings:

HP 71600 Series	Explains that the HP 71600 Series is a Modular Measurement System (MMS), introduces the MMS master/slave concept and lists MMS terms. The MMS master/master concept is explained in *Appendix A*.
HP-MSIB	Covers the topics you need to know when connecting to the Hewlett-Packard Measurement System Interface Bus (HP-MSIB).

HP 71600 Series

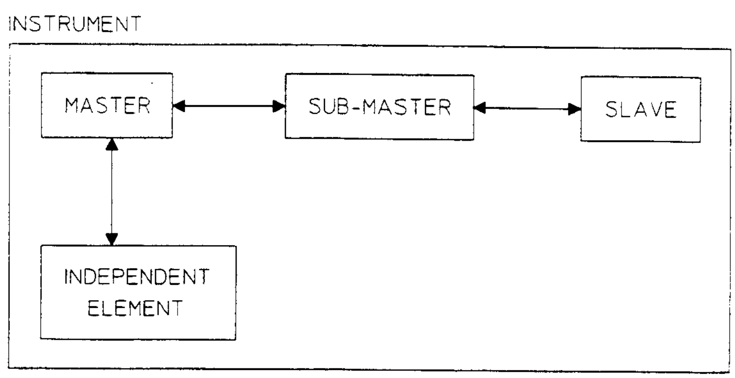
The basic master/slave MMS model and how it relates to the HP 71600 Series is described under the following headings:

- Basic Master/Slave MMS Model
- Communicating within an MMS
- HP 71600 Series with MMS Terms

Note For master/master MMS configuration, see *Appendix A*.

Basic Master/Slave MMS Model

The basic master/slave model is illustrated in the following diagram.



The master in the above diagram communicates to the other elements in the system as follows:

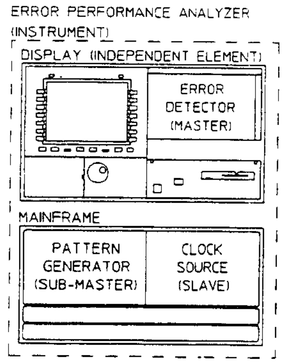
Master communicates directly with the sub-master.
Master communicates with the slave through the sub-master.
Master communicates directly with the independent element.
Sub-master communicates with slave.

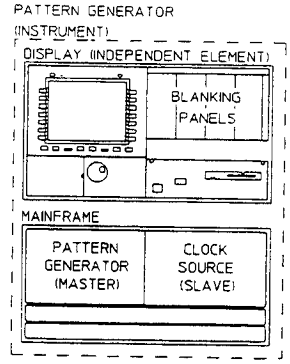
The terms used in the MMS are described on the next page.

MMS Terms	Description
Functional Terms	
Element	Any device that can communicate over the HP-MSIB.
Instrument	Any element or group of elements that perform an independent function (for example, the HP 71603B 0.1-3 Gbit/s Error Performance Analyzer).
Master	An element that can control slaves over the HP-MSIB.
Sub-master	An element that simultaneously controls other elements and is itself controlled by another element.
Slave	An element that is currently controlled by another element.
Independent Element	An element that is neither a master or slave (for example the HP 70004A Display).
Hardware Terms	
Mainframe	A device into which plug-in modules are installed. An MMS instrument is made up of one or more modules installed into a mainframe.
Module	A device that plugs into a mainframe. Modules cannot operate unless they are installed into a mainframe. Modules are designed in various widths described as either a 1/8-width, 2/8-width, 3/8-width or 4/8-width module.
Stand-alone Instrument	An element capable of performing its functions without a mainframe.
Extender Module	This module contains an HP-MSIB extender cable which is used when an element is being worked on outside the mainframe.
User Terms	
Address Map	A graphic representation (row, column) of assigned and available HP-MSIB addresses. It is also a matrix that represents the relationship among master, slave and independent elements (see page 6-6).
Address Switches	These switches set the HP-MSIB addresses of modules and also set the HP-IB addresses of modules in *row 0*.
HP-MSIB Row 0	Modules assigned to row 0 report all errors to the display. Only row 0 modules can have *HP-IB* addresses. When you select the *NEXT INSTR* display function, the display searches row 0 only.
Error Messages	These are coded messages used to indicate module or system status. These codes are identified in *Troubleshooting*.

HP 71600 Series with MMS Terms

The basic HP 71600 Series configurations with MMS terms highlighted in parenthesis are illustrated in the following diagrams:





Your system is shipped to you from the factory as a master/slave Modular Measurement System (MMS).

In an Error Performance Analyzer system the Error Detector master module controls the slave Pattern Generator and Clock Source modules. The Pattern Generator module (a slave to the Error Detector) is a sub-master to the Clock Source. The Clock Source is controlled directly by the Pattern Generator, and indirectly by the Error Detector (through the Pattern Generator).

In a Pattern Generator system the master module is the Pattern Generator, it controls the slave Clock Source module.

Communicating within an MMS

Elements which make up an MMS, communicate over the Hewlett-Packard Measurement System Interface Bus (HP-MSIB). To communicate successfully:

- Ensure the cabling is correct, see page 2-13.
- Ensure the addresses assigned to the elements that make up your system follow the protocol outlined in the HP-MSIB section, see page 6-6. The factory preset addresses are shown on page 6-5.

Hewlett-Packard Measurement System Interface Bus (HP-MSIB)

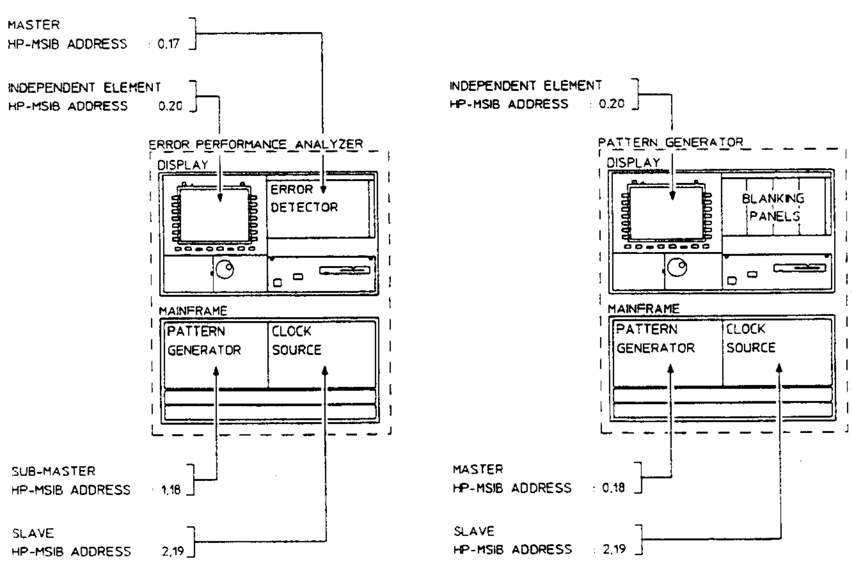
This section details information required to help you with HP-MSIB:

- Preset Addresses
- Changing Addresses
- Assigning Addresses
- Basic HP-MSIB Cabling
- HP 71600 Series HP-MSIB Cabling

Preset Addresses

The MMS uses an address map (or matrix) of 8-rows and 32-columns to enable you to assign addresses to elements in your system.

The HP 71600 Series HP-MSIB factory preset addresses (row, column) are shown in the following diagram:



Changing Addresses

Ensure you are fully aware of your system in relation to the MMS address protocol when assigning addresses or the system will fail to operate (see page 6-6).

All elements which communicate over the HP-MSIB have address switches (typically 8 switches in the one package):

Three switches define the row address
Five switches define the column address

The system must be powered down when you change the address settings. The switches are read at power-on (for more information on the *Address Switches*, see page 2-7).

Assigning Addresses (in a master/slave configuration)

Note For master/master configuration information, see *Appendix A*.

There is a protocol which must be adhered to when assigning addresses to elements in a Modular Measurement System (MMS). The protocol for assigning addresses to master, sub-master, slave modules and independent elements in an MMS is explained in the following pages.

The MMS uses an address map (or matrix) of 8-rows and 32-columns to enable you to assign addresses to the elements in your system.

Note There are 255 possible addresses available. Row 0, column 31 is not a valid address.

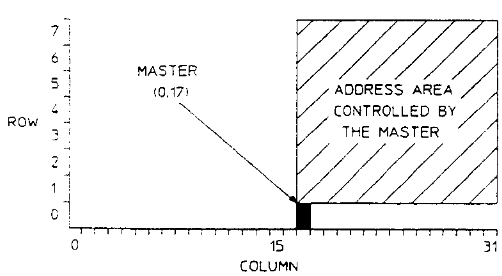
Addresses cannot be assigned indiscriminately - rules have to be followed:

1. Assign the master module address (row, column) - the master must be assigned to *row 0* if you want your system to communicate over the HP-IB, or if you want to use the Display *REPORT ERRORS* function.

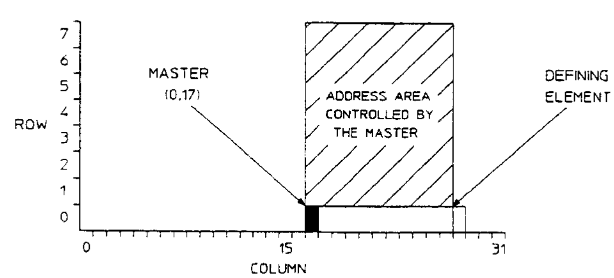
   Each master has a slave address area, any module in that area may be controlled by the master. The boundaries of the slave address area are defined as follows:

Row Boundaries	The first boundary is the row immediately above the master, the other boundary is row 7 (see the following diagram). If the master is located in *row 7*, it cannot have slaves.
Column Boundaries	The first boundary is the same column as the master. The other boundary is column 31 or any column to the right of the master containing a module (this is known as a defining element) which has a *row* address at or below the master row. The column containing the defining element is not part of the slave address area.

   The following diagrams show the slave address area of a system with and without a defining element.



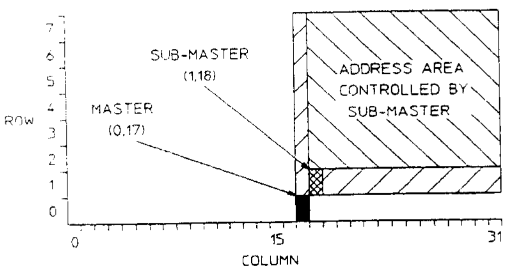
Without a Defining Element



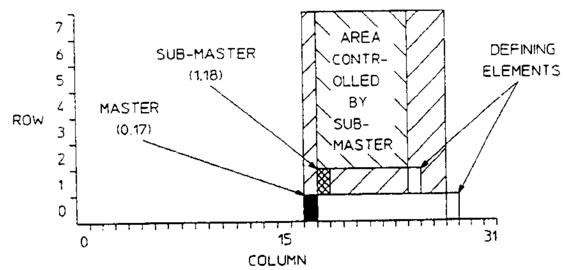
With a Defining Element

2. Assign the sub-master module address - any row and column within the control of the master, see the previous diagrams.

   The slave address area controlled by the sub-master is determined by the addresses of the sub-master the defining element - if your system has one (see previous step for *row* and *column* boundaries). The following diagrams show the slave address area of a system with and without defining element.



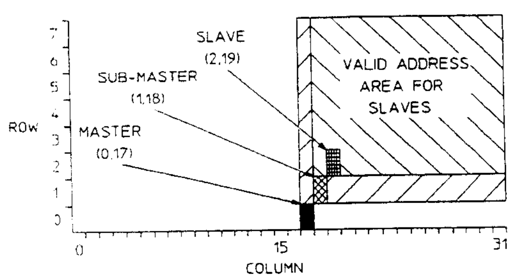
Without Defining Elements



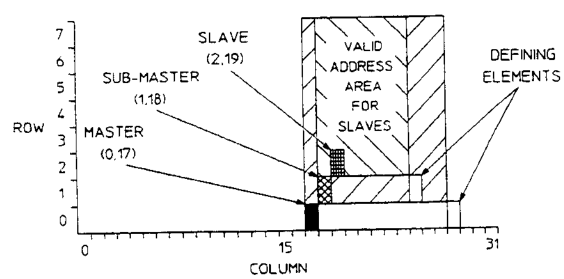
With Defining Elements

Note The slave address area of the sub-master is excluded from the slave address area of the master.

3. Assign the slave address - any row and column within the control of the master or sub-master. The following diagram shows the slave in the sub-master slave address area. The master can only communicate with this slave through the sub-master.



Without Defining Elements



With Defining Elements

Slave Area and Defining Elements

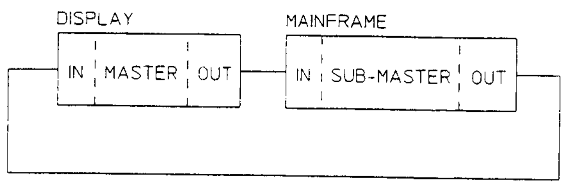
Master modules establish their slave address area by determining the location of a defining element (if the system has one). The master address and the defining element address establish the slave area boundaries.

The address requirements of a defining element are as follows:

$$\text{Column Address} > \text{the column address of the master (or sub-master)}$$
$$\text{Row Address} \leq \text{the row address of the master (or sub-master)}$$

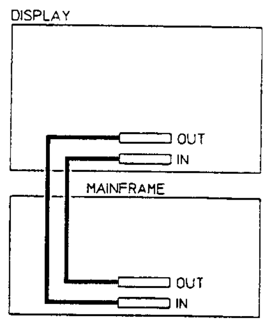
Basic HP-MSIB Cabling

An MMS requires that the HP-MSIB cables which interconnect the Display and Mainframe form a closed loop, see the diagram below:



HP 71600 Series HP-MSIB Cabling

The following diagrams show the HP-MSIB cabling for your system. The connectors are located on the Display, Mainframe and Clock Source.



The diagram shows the systems viewed from the rear.

7

Hewlett-Packard Interface Bus (HP-IB)

The HP 71600 Series can be controlled remotely by an external controller over the HP-IB. This section contains information to help you with HP-IB:

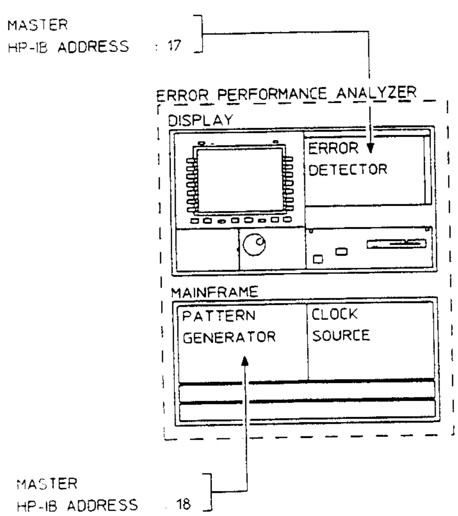
- Preset Addresses
- Changing Addresses
- Assigning Addresses
- Connecting your system to an HP-IB controller
- Cables and Connectors

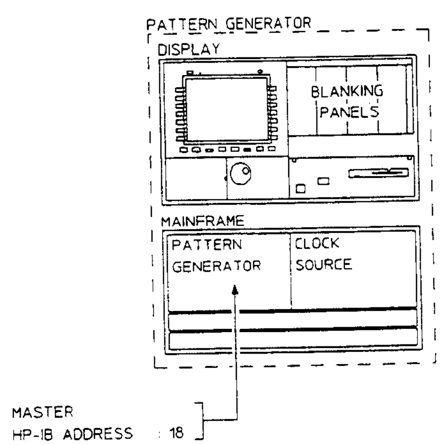
Preset Addresses

The HP 71600 Series factory preset HP-IB addresses are shown in the following diagram:

Note

Ensure that the Error Detector and Pattern Generator module *row addresses* are set to *0* for HP-IB operation.





Changing Addresses

The recommended method of changing the HP-IB address (*column address*) of your master module is to use the *HP-IB Address* function on the Display, see the *HP 71600 Series Operating Manual*.

The system normally powers on with the HP-IB address established before the last power down. However, if you change the *column* settings of the HP-MSIB/HP-IB switches the system will power up with the value.

Caution It is not recommended that you change the HP-IB address using the HP -MSIB/HP-IB switch, as this also changes the HP-MSIB address. If the HP-MSIB address protocol is violated your system will fail to operate.

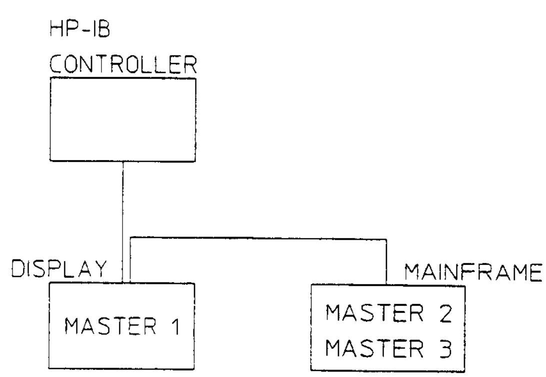
Assigning Addresses

An HP-IB address can only be assigned to an element in *row 0* - normally the master element in your system.

Cabling (HP-IB)

The number of HP-IB cables required is dependent on the numberof displays and mainframes, and on how the masters are distributed in your system.

For example, if a three master system has one master housed in a display and the other two housed in a mainframe, then two cables are required - from the HP-IB controller to the display, the other from the display to the mainframe, see the diagram below:



Connecting Your System to an HP-IB Controller

Your System can be controlled by an external controller through the HP-IB. Only one cable is required for a *Pattern Generator* system, it is connected to the Display. Two cables are required for the *Error Performance Analyzer* system.

For more details on remote control, see *HP 71600 Series Operating Manual*.

HP-IB Connector Pinout and Cables

The connector pinout and the cable HP part numbers of suitable cables are shown below:

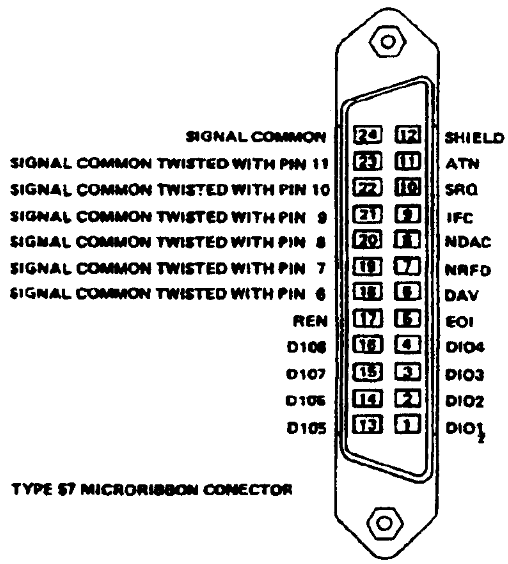
Logic Levels

The HP-IB logic levels are TTL compatible i.e. the true (1) state is 0 to +0.5V DC and the false (0) state is +2.5 to +5V DC.

Mating Connector

HP 1251-0293;
Amphenol 57-302040

HP Part Number	Cable Length
HP 10833A	1 m (3.3 ft)
HP 10833B	2 m (6.6 ft)
HP 10833C	4 m (13.2 ft)
HP 10833D	0.5 m (1.6 ft)



A

Master/Master Configuration

Introduction

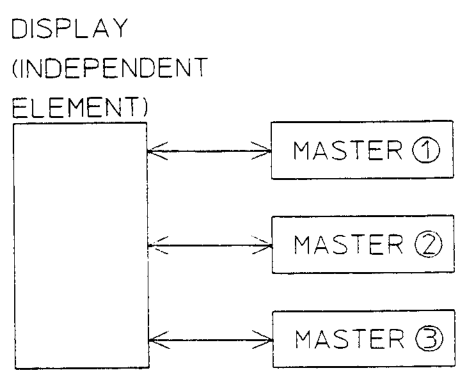
A Modular Measurement System (MMS) master/master configuration is where two or more modules are assigned as masters (have addresses on row 0).

In an MMS master/master setup each master element operates and communicates independently with the Display. Master/master information is covered under the following headings:

- Basic Master/Master Configuration
- Assigning Addresses (HP-MSIB)
- Cabling (HP-MSIB)
- HP 71600 Series in a Master/Master Configuration
- Assigning Addresses (HP-IB)
- Cabling (HP-IB)

Basic Master/Master Configuration

A typical master/master configuration is shown in the following diagram:

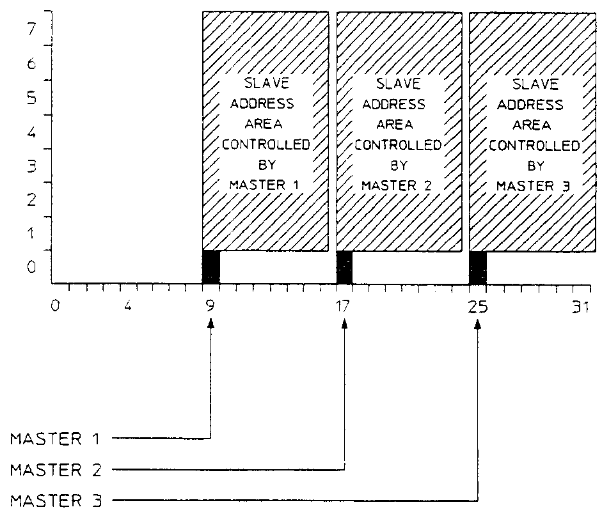


In a master/master configuration, the Display is connected to two or more masters. However, only one master can be in control of the display at a time. This master communicates with the slave(s) that it controls and the display. Masters do not communicate with each other.

Assigning Addresses (HP-MSIB)

Assigning HP-MSIB addresses in a master/master configuration is similar to the master/slave explained on page 6-6.

The addressing is based on a map or matrix of 8-rows and 32-columns. A typical map (for the 3-master system shown in the previous diagram) is shown below:



Note

Only one master at a time can communicate with the display.

The diagram shows that the addresses assigned to each master affects the number of slave addresses available to each master:

The address of Master 2 defines the number of slave addresses (address area) available to Master 1.

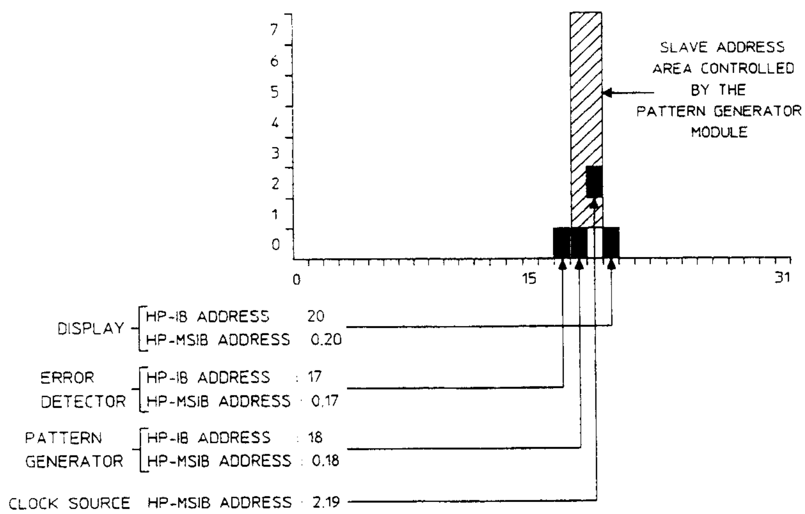
The address of Master 3 defines the number of slave addresses (address area) available to Master 2.

Cabling (HP-MSIB)

HP-MSIB cabling is similar to master/slave configuration, see page 6-8.

HP 71600 Series in a Master/Master Configuration

A typical address map for *Error Performance Analyzers* in a master/master configuration is shown below, both HP-MSIB and HP-IB addresses are shown.



B

Instrument Operation

Introduction

This appendix contains operating information which is specifically required for the *Performance Tests* in chapter 4. For a wider coverage of instrument operation see *HP 71600 Series Operating Manual.*

The operating tasks covered are listed below:

Set the Data Amplitude and Hi-Level

Set the Clock Output Level

Set up and Transmit a User Pattern

Set the Data Output Delay

Transmit an Alternate Word

To Format a Disc

1. Insert an unformatted disc into the disc drive.
2. Press the (MENU) key, then select the left-menu `misc` softkey.
3. Press the right-menu `format disc` softkey.

Note Ensure the disc you place in the disc drive is unformatted. The `format disc` function will erase the contents of a formatted disc.

To Delete a Disc Pattern

1. Repeat the previous three steps, then press `delete discpat`. Delete a pattern by selecting the appropriate `DISC PATT` softkey.

To set the Data Amplitude and Hi-Level

1. Press `data o/p err-add`.
2. Select `DATA AMPLTD` then use either the rotary knob or the numeric keys to set the value.

   If you use the rotary knob the units (mV or V) are automatically selected. If you use the numeric keys, the units must be selected from the keys to the right of the display (mV, V or CLEAR).
3. Select `DATA HI-LEVL` then use the rotary knob or numeric keys to set the value.

Note The `DATA HI-LEVL` is the voltage set for the top of the data pulse.

To set the Clock Output Level

1. Press `trg o/p clk o/p`.
2. Select `CLOCK AMPLTD` then use either the rotary knob or the numeric keys to set the value.

   If you use the rotary knob the units (mV or V) are automatically selected. If you use the numeric keys, the units must be selected from the keys to the right of the display (mV, V or CLEAR).

To Set up and Transmit a User Pattern

Setting up a User Pattern

1. Press `edit usr-pat`.
2. Select from `INTERNL PATT`, `DISC PATT` or `CURRENT PATTERN`. If you want to modify the current pattern, select `CURRENT PATTERN` then use the softkeys on the `more 1 of 3` and `more 2 of 3` right-menus to edit the current pattern.

To Set Pattern Length

3. Select the `more 2 of 3` right-menu and press `set pat length`, then use the numeric keys to set the pattern to the desired length and press `ENTER`.
4. Use the 0 and 1 keys (as required) to enter the pattern. The rotary knob may be used to scan the pattern.

To Load and Modify a PRBS or User Pattern

The editor load block function enables the user to load one of four fixed PRBS's, or the contents of a user pattern store into the *user pattern memory* at the current cursor position. The current setting of the `INSERT/REPLACE` softkey (on the `more 1 of 3` right-menu) determines whether the contents of the PRBS or pattern store (the block) are inserted into, or replace bits in the pattern.

The number of block bits loaded from the PRBS or pattern store is tailored to fit between the cursor and pattern end. For example if the cursor is sitting on bit 500 of a 900 bit pattern, then when a block load is performed up to 400 bits can be inserted/replaced.

5. Set the cursor to the bit in the pattern where you wish to insert/replace a block of data. Use the display knob or `goto bit` softkey.
6. Set the `INSERT/REPLACE` softkey to the desired mode.
7. Select the `more 2 of 3` right-menu.
8. Select `load block` - the right-menu changes to give a sub-menu set of softkeys, offering the choice of selecting a fixed PRBS of 2^7, 2^{10}, 2^{11} or 2^{13}, or a `user pattern`. For this procedure, select a PRBS.
9. When you select a PRBS the right-menu changes to give softkeys of `NO MODIFY`, `zero sub`, `mark density` and `CANCEL LOAD`.

   If you do not wish to edit zero substitution or mark density, press `NO MODIFY`.

To Save a Pattern

10. To save the pattern you have selected and edited, select the `more 1 of 3` right-menu and press `save pattern`.
11. Select the `INTERN PATT` or `DISC PATT` store into which you wish to save the current pattern.

To Transmit a User Pattern

12. Press `select pattern` followed by `user pattern`.
13. Select the pattern you want to transmit `INTERNL PATT` or `DISC PATT`.

Note You may edit a User Pattern while it is being transmitted (ACTIVE). If you do this, the transmitted pattern will change immediately the 0 or 1 keys are pressed in step 4.

To Set the Data Output Delay

1. Press data o/p err-add.

2. Select DAT O/P DELAY then use either the rotary knob or the numeric keys to set the value.

   If you use the rotary knob the units (ns or ps) are automatically selected. If you use the numeric keys, the units must be selected from the keys to the right of the display (ns, ps or CLEAR).

To Transmit an Alternate word

1. Press select pattern followed by more 1 of 3 then press alt words. The alternate word is now being transmitted (Active).

   To Edit the Alternate Word

2. Press alt words again.

3. Select ENTER WORD 0 then use numeric keys 0 and 1 to edit the sixteen bit pattern. Press ENTER to store the new pattern.

4. Select ENTER WORD 1 then use numeric keys 0 and 1 to edit the sixteen bit pattern. Press ENTER to store the new pattern.

5. Press EXIT.

Note

The Alternate Word transmitted (WORD 0 or WORD 1) depends on the state of the *AUX INPUT* on the rear panel of the Pattern Generator. If no input is connected, WORD 1 only is transmitted.

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71600-90005
Edition 3

Printed in U.K.